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(54)   **Method and apparatus for fabricating self-assembling microstructures**

(57)   A method and apparatus for assembling micro-structures onto a substrate through fluid transport. The microstructures being shaped blocks self-align into recessed regions located on a substrate such that the microstructure becomes integral with the substrate. The improved method includes a step of transferring the shaped blocks into a fluid to create a slurry. Such slurry is then dispensed evenly or circulated over the top surface of a substrate having recessed regions thereon. The microstructure via the shape and fluid tumbles onto the surface of the substrate, self-aligns, and engages into a recessed region.
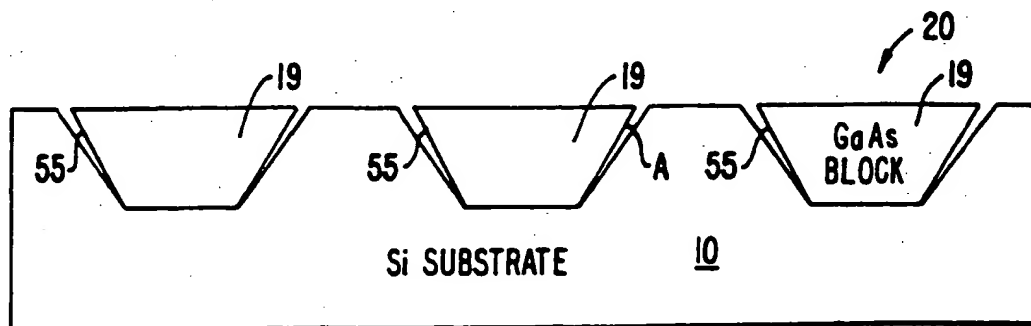
FIG. 7.

EP 0 747 948 A2

Description

GOVERNMENT RIGHTS NOTICE

This invention was made with government support under Grant (Contract) Nos. AFOSR-91-0327 and F49620-92-J-054-1 awarded by the Department of Defense. The Government has certain rights to this invention.

BACKGROUND OF THE INVENTION

The present invention relates to the field of electronic integrated circuits. The invention is illustrated in an example with regard to the manufacture of gallium arsenide microstructures onto a silicon substrate, but it will be recognized that the invention will have a wider range of applicability. Merely by way of example, the invention may be applied in the manufacture of devices containing silicon based electronic devices integrated with a gallium arsenide based microstructures (or devices) such as light emitting diodes (LED), lasers, tunneling transistors, Gunn oscillators, integrated circuits, solar collectors, liquid crystal displays (LCDs), and others.

Industry currently needs a cost effective, efficient, and practical method for assembling a higher cost microstructure onto a lower cost commercially available substrate. In particular, a material such as gallium arsenide possesses substantially better characteristics for some specific electronic and opto-electronic applications rather than materials such as silicon. However, in the fabrication of gallium arsenide devices, substantial regions of a gallium arsenide wafer are typically unused and wasted. Such unused regions generally create an inefficient use of precious die area. In addition, processing gallium arsenide typically requires special techniques, chemicals, and equipment, and is therefore costly.

Other applications such as very large scale integrated (VLSI) circuits may he better fabricated in silicon rather than gallium arsenide. In still further applications, it may be desirable to produce integrated circuits having characteristics of both types of materials. Accordingly, industry needs to develop an effective method of fabricating a gallium arsenide device integrated with a silicon based integrated circuit. The resulting structure of such method includes advantages of both gallium arsenide and silicon based devices.

Methods such as flip chip bonding, lift off methods, and others, generally require large areas of a substrate and are incompatible with a micron sized state-of-art microstructure. Such methods often create difficulty in positioning a particle onto a substrate. Accordingly, industry needs to develop an effective method of fabricating higher cost materials such as a gallium arsenide microstructure onto a lower cost substrate such as silicon.

Industry utilizes or has proposed several methods for fabricating individual electronic components (or generally microstructures) and assembling such structures onto a substrate. One approach is to grow gallium arsenide devices directly onto a silicon substrate. This approach becomes limiting because the lattice structure of gallium arsenide mismatches that of silicon. In addition, growing gallium arsenide onto silicon is inherently difficult and therefore costly. Accordingly, gallium arsenide can not efficiently be grown on a silicon substrate.

Another approach is described by Yando in U.S. Patent No. 3,439,416. Yando describes components or structures placed, trapped, or vibrated on an array of magnets. Such magnets include magnetized layers alternating with non-magnetized layers to form a laminated structure. Components are matched onto the array of magnets forming an assembly thereof. However, severe limitations exist on the shape, size, and distribution of the components. Component width must match the spacing of the magnetic layers and the distribution of components are constrained by the parallel geometry of lamination. In addition, self-alignment of components requires the presence of the laminated structure. Furthermore, the structures disclosed by Yando typically possess millimeter sized dimensions and are therefore generally incompatible with micron sized integrated circuit structures. Accordingly, the method and structure disclosed by Yando is thereby too large and complicated to be effective for assembling a state-of-art microstructure or component onto a substrate.

Another approach involves mating physical features between a packaged surface mount device and substrate as described in U.S. Patent No. 5,034,802, Liebes, Jr. et al. The assembly process described requires a human or robotics arm to physically pick, align, and attach a centimeter sized packaged surface mount device onto a substrate. Such process is limiting because of the need for the human or robotics arm. The human or robotics arm assembles each packaged device onto the substrate one-by-one and not simultaneously, thereby limiting the efficiency and effectiveness of the operation. Moreover, the method uses centimeter sized devices (or packed surface mount integrated circuits), and would have little applicability with micron sized integrated circuits in die form.

Another approach, such as the one described in U.S. Patent No. 4,542,397, Biegelsen et al. involves a method of placing parallelogram shaped structures onto a substrate by mechanical vibration. Alternatively, the method may also employ pulsating air through apertures in the support surface (or substrate). A limitation to the method includes an apparatus capable of vibrating the structures, or an apparatus for pulsating air through the apertures. Moreover, the method described relies upon centimeter-sized dies and would have little applicability with state-of-art micron sized structures.

A further approach such as that described in U.S. Patent No. 4,194,668 by Akyurek discloses an apparatus for aligning and soldering electrode pedestals onto

solderable ohm... anode contacts. The anode contacts are portions of individual semiconductor chips located on a wafer. Assembling the structures requires techniques of sprinkling pedestals onto a mask and then electromagnetic shaking such pedestals for alignment. The method becomes limiting because of the need for a shaking apparatus for the electromagnetic shaking step. In addition, the method also requires a feed surface gently sloping to the mask for transferring electronic pedestals onto the mask. Moreover, the method is solely in context to electrode pedestals and silicon wafers, thereby limiting the use of such method to these structures.

Still another approach requires assembling integrated circuits onto a substrate through electrostatic forces as described in Application Serial No. 07/902,986 filed June 23, 1992 by Cohn. The electrostatic forces vibrate particles such that the particles are arranged at a state of minimum potential energy. A limitation with such method includes providing an apparatus capable of vibrating particles with electrostatic forces. Moreover, the method of Cohn creates damage to a portion of the integrated circuits by mechanically vibrating them against each other and is also generally ineffective. Accordingly the method typically becomes incompatible with a state-of-art microstructure.

From the above it is seen that a method of assembling a microstructure onto a substrate that is compact, low cost, efficient, reliable, and requires little maintenance is desired.

SUMMARY OF THE INVENTION

The present invention pertains to a method and resulting structure for assembling a microstructure onto a substrate. In particular, the method includes transferring shaped blocks or generally structures via a fluid onto a top surface of a substrate having recessed regions or generally binding sites or receptors. Upon transferring, the blocks self-align through their shape into the recessed regions, and integrate thereon. The resulting structure may include a variety of useful electronic integrated circuits containing silicon based electronic devices integrated with a gallium arsenide based microstructures such as a light emitting diodes (LED), lasers, tunneling transistors, Gunn oscillators, integrated circuits, solar collectors, and others. As an additional example, semiconductor devices may be integrated with other semiconductor devices or other substrate materials, such as plastic.

In one specific embodiment, the method provides assembling a microstructure such as a micron sized block onto a substrate. The substrate includes a top surface with at least one recessed region thereon and may be either a silicon wafer, gallium arsenide wafer, glass substrate, ceramic substrate, or others. The substrate may also be a plastic sheet fabricated from a technique such as stamping, injection molding, among others. Assembling steps include providing shaped blocks, and

transferring the blocks into a fluid to form a mixture thereof or generally a slurry. Such slurry is then dispensed evenly over the substrate at a rate where at least one of the shaped blocks is disposed into a recessed region. Dispensing occurs at substantially a laminar flow and allows a portion of the shaped blocks to self-align into the recessed region. Alternatively, the method includes circulating the slurry at a rate where at least one of the shaped blocks is disposed into a recessed region. A gas, including but not limited to nitrogen, facilitates circulation of the slurry and allows a portion of the shaped blocks to self-align into the recessed regions.

The invention further provides related apparatus for assembling a microstructure on a substrate with at least one recessed region thereon. The apparatus includes a vessel that contains the substrate, a fluid, and the shaped blocks. The apparatus also includes a pump that circulates the shaped blocks within the vessel at a rate where at least one of the shaped blocks is disposed into a recessed region.

In an alternative embodiment, the method provides, for example, shaped blocks having a trapezoidal profile from an improved fabrication process. Fabrication includes providing a second substrate having a top surface, and growing a sacrificial layer overlying the top surface. A step of forming a block layer overlying the top surface is then performed. Masking and etching the block layer up to the sacrificial layer creates trapezoidal shaped blocks thereon. A step of preferential etching the sacrificial layer lifts off each trapezoidal shaped block. Such blocks are then rinsed and transferred into a solution forming the slurry. In this embodiment, the method provides alternate fabrications of the shaped blocks. One such alternate fabrication of the shaped blocks includes providing a second substrate as a block layer having an upper surface and a bottom surface, and growing a sacrificial layer overlying the upper surface. Another alternative fabrication of the shaped blocks includes providing a second substrate having an upper surface, a sacrificial layer overlying the upper surface, and a block layer overlying the sacrificial layer. After providing the second substrate, a step of forming trapezoidal shaped blocks on and in contact with the sacrificial layer is then performed. The trapezoidal shaped blocks are then removed from contact with the sacrificial layer, and transferred into a fluid to form a slurry.

The invention further provides a resulting trapezoidal shaped block integral with a substrate. The substrate includes a plurality of recessed regions thereon. Each recessed region includes a shaped profile to accept a trapezoidal shaped block. The resulting structure has such blocks integrated with the substrate via the recessed regions forming assembled devices or integrated circuits.

Still a further embodiment, the shaped block comprises a truncated pyramid shaped gallium arsenide structure. The truncated pyramid shaped structure

includes a base with four sides protruding therefrom to a larger top surface. Each side creates an angle between about 50° and about 70° from the base to a side. Each side may also have a height between about 5 μm and about 15 μm. The block may have a length between about 10 μm and about 50 μm, and a width between 10 μm and about 50 μm.

An alternative embodiment provides a method of forming a hybrid integrated circuit. The present method includes providing a first tapered shaped block that includes a first electronic device portion thereon, and a second electronic device portion. The present method also includes placing the first shaped block into a first recessed region of a substrate. A step of interconnecting the first shaped block with the second electronic device portion is also included. The interconnecting step is a metallization step.

The improved method and resulting structure are in context to a trapezoidal shaped block made of gallium arsenide assembled onto a silicon substrate merely for illustrative purposes only. The improved method and related apparatus are in context to different sized trapezoidal shaped blocks made of silicon assembled onto a silicon substrate merely for illustrative purposes. The shaped blocks may also include a cylindrical shape, pyramid shape, rectangular shape, square shape, T-shape, kidney shape, or the like (symmetrical and asymmetrical), and combinations thereof. Generally, the shape of the block allows the block to closely insert into a similarly shaped recessed region or receptor on a substrate. The shaped blocks also comprise a material such as gallium aluminum arsenide, silicon, diamond, germanium, other group III-V and II-VI compounds, multilayered structures, among others. Such multilayered structure may include metals, insulators such as silicon dioxide, silicon nitride, and the like, and combinations thereof.

A further understanding of the nature and advantages of the invention will become apparent by reference to the remaining portions of the specification and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a gallium arsenide wafer having a molecular beam epitaxy (MBE) grown gallium arsenide layer for the improved method of fabrication;

Fig. 2a is an illustration of trapezoidal shaped gallium arsenide blocks etched from an MBE grown gallium arsenide layer;

Fig. 2b is an illustration of reverse trapezoidal shaped blocks;

Fig. 3 is an illustration for a lift-off step of gallium arsenide blocks;

Fig. 4 is an illustration of a portion of an alternative lift-off step using a intermediate substrate;

Fig. 5 is an illustration of another portion of the alternative lift-off step of Fig. 4;

Fig. 6 is an illustration of each gallium arsenide block self-aligning onto a silicon substrate;

Fig. 7 is an embodiment of a microstructure assembled onto the silicon substrate according to the improved method depicted by Figs. 1-3 and 6;

Fig. 8 is an alternative embodiment of a microstructure assembled onto a substrate;

Fig. 9 is an embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode;

Fig. 10 is an alternative embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode;

Fig. 11 is a further alternative embodiment of a microstructure assembled onto a substrate forming a gallium arsenide diode;

Fig. 12 is an illustration of examples of shaped blocks;

Fig. 13 is a photograph of an assembled microstructure according to the experiment; and

Fig. 14 is a photograph of an operational photo diode according to the experiment.

Fig. 15 is a photograph of a metallized ring layer overlying a gallium arsenide block;

Fig. 16 is a current-voltage representation for a gallium arsenide diode according to the experiment;

Fig. 17 is a current-voltage representation for a gallium arsenide/aluminum arsenide resonant-tunneling diode according to the experiment;

Fig. 18 is a silicon wafer having a deposited silicon nitride layer for an alternate improved method of fabrication of shaped blocks;

Fig. 19 is a silicon-on-insulator wafer having a silicon-on-insulator layer overlying an insulator layer overlying a silicon substrate for another alternate improved method of fabrication of shaped blocks;

Fig. 20 is an illustration of a mask used to fabricate silicon shaped blocks; and

Fig. 21 is an illustration of an apparatus for assembling microstructures onto a substrate.

DESCRIPTION OF SPECIFIC EMBODIMENTS

With reference to Figs. 1-21, the present invention provides an improved method of fabricating a microstructure onto a substrate, a related apparatus, and an improved resulting structure. Figs. 1-17 are, for example, in context to fabricating and assembling a shaped gallium arsenide block onto a silicon substrate for illustrative purposes only. Figs. 18-21 are, as further examples, in context to fabricating and assembling shaped silicon blocks onto a silicon substrate for illustrative purposes only.

In the assembly of a gallium arsenide block onto a silicon wafer, trapezoidal shaped blocks self-align into inverted trapezoidal shaped recessed regions located on the top surface of the silicon wafer. Steps for such method include forming the gallium arsenide blocks, transferring the blocks into a solution forming a slurry, and spreading the slurry evenly over the top surface of

a silicon substrate having recessed regions. During the spreading steps, the blocks self-align and settle into the recessed regions while being transported with the fluid across the top surface. Optionally, the slurry is spread evenly over the top surface of a silicon substrate by way of mechanical means such as a brush, a scraper, tweezers, a pick, a doctor blade, and others. The mechanical means may be used to move or distribute the slurry and also to remove excess slurry. As an alternative to spreading the slurry, the method includes circulating the slurry over the top surface of the substrate having recessed regions. During the circulating step, the blocks self-align and settle into the recessed regions while being transported with the fluid across the top surface. The blocks which do not settle into recessed regions are then recirculated until a certain fill-factor is achieved. Of course, the mechanical means may also be used in conjunction with the circulating step. The details of fabricating the silicon substrate having recessed regions will be discussed in detail below after a brief discussion of forming the gallium arsenide blocks. Details of the method using the circulating step and related apparatus will be discussed in detail below after a discussion of fabricating the silicon substrate having recessed regions.

In a specific embodiment, the method provides as an example a step of forming trapezoidal shaped blocks from a gallium arsenide wafer. It should be noted that the shaped blocks are also micromachined structures or the like. Such step includes providing a gallium arsenide wafer 10 as illustrated in Fig. 1. The method also provides forming sacrificial layer 13 by chemical vapor deposition, sputtering, or the like overlying top surface 15 of gallium arsenide wafer 10. Such sacrificial layer 13 includes, for example, aluminum arsenide. Other sacrificial layers may include indium phosphate, silicon dioxide, photoresist, among other materials capable of being selectively etched. Of course, the sacrificial layer used depends upon the particular application. For an aluminum arsenide sacrificial layer, thickness for such layer is between about 0.1 μm and about 5.0 μm, and preferably at about 1 μm. Before forming sacrificial layer 13, a step of etching top surface 15 by methods such as wet etching, plasma etching, or reactive ion etching clears off any native oxide. Alternatively, a step of desorption in the presence of arsenic removes the native oxide layer. A subsequent step of preferential etching (to be discussed in detail later) removes sacrificial layer 13 to facilitate the lift-off of each gallium arsenide block (also called a mesa shaped or trapezoidal shaped or truncated pyramid shaped structure) formed overlying sacrificial layer 13.

In Fig. 1, gallium arsenide layer 17 forms overlying sacrificial layer 13. Such gallium arsenide layer may be fabricated by methods including molecular beam epitaxy, chemical vapor deposition, and others. The thickness (T) of the gallium arsenide layer is at least about 10 nm and greater, and preferably at about 10 μm and greater, depending upon the particular application.

To produce the desired dimensions for the block, the improved method provides the steps of masking and etching gallium arsenide layer 17. Fig. 2a illustrates gallium arsenide substrate 10 after such masking and etching steps and includes gallium arsenide blocks 19 and a photoresist layer 21 overlying gallium arsenide layer 17 (not shown). Generally, unexposed portions of gallium arsenide layer 17 are etched up to sacrificial layer 13 as illustrated in Fig. 2a. Such etching step provides a plurality of shaped gallium arsenide blocks 19. For the present example, the shaped blocks include a trapezoidal profile or truncated pyramid shape. Such trapezoidal profile may be fabricated by methods of wet etching, plasma etching, ion milling, reactive ion etching, among others, depending on the application.

Generally, a wet etch produces a sloping profile along the sides or edges of each gallium arsenide block. For mask edges parallel to the [1$\bar{1}$0] direction, a wet etch produces an outward sloping profile as illustrated in Fig. 2a. Alternatively, mask edges parallel to the [110] direction, produces an inward sloping (or reverse mesa) profile. The outward sloping profile provides a desired shape which integrates into a silicon substrate having recessed regions shaped in a complementary manner.

Ion milling produces gallium arsenide blocks with outward sloping profiles, depending upon the beam angle. Beam angle is adjusted between about 0° to about 30° from a normal to top surface 15 on gallium arsenide substrate 10. To create the outward sloping (or truncated pyramid shape) profile for each block, the entire structure is typically rotated during such etching step.

Reactive ion etching (RIE) also produces blocks having a shaped profile in many materials such as gallium arsenide, silicon, or others. In general, a vertical etch may be used at a tilt to cut each sidewall angle. A substantially vertical etch process may also be tuned to undercut at a selected angle without tilting the substrate. In addition, a vertical etch or a reactive ion etch may be used in combination with a wet chemical etch to provide the undercut. Such etching methods create blocks having undercut sides or a reverse mesa profile, as shown in Fig. 2b. Fig. 2b illustrates reverse trapezoidal shaped blocks. Fig. 2b shows substrate 925 (of material such as gallium arsenide, silicon, or the like) after such masking and etching steps and includes shaped blocks 929 on a sacrificial layer 927. A mask layer 933 overlies a device layer 931 which includes electronic or other devices or portions of devices. Generally, unexposed portions of block layer 929 are etched through sacrificial layer 927 as illustrated in Fig. 2b. Depending upon variables such as the etchant, pressure, equipment, and others, such etching method may create blocks having substantially consistent shapes and/or profiles. Vertical etches and wet etches may be used or combined to produce such reverse mesa profiles. A plurality of shaped blocks 929 are thereby produced by removal of the sacrificial layer 927. Removal of the sacrificial layer 927 may be accomplished for

example by selective etching, chemical conversion (such as preferentially oxidizing the sacrificial layer, preferentially converting the sacrificial layer into porous Silicon, or others) followed by selective etching, thermal or ultrasonic or mechanical fracture, or dissolving, among others, and preferably by selective etching. Alternatively, the functionality of the sacrificial layer 927 may be included in the substrate 925, separating the blocks 929 by removal or etching of substrate 925 in whole or in part.

In a specific embodiment, after etching the MBE grown layer, trapezoidal shaped blocks are removed through a lift-off technique from gallium arsenide substrate 10 by preferential etching sacrificial layer 13 as illustrated in Fig. 3. Such lift-off technique occurs by, for example, a preferential wet etch of the aluminum arsenide sacrificial layer. In the gallium arsenide example, such wet etching step is typically performed by a chemical such as a hydrofluoric acid solution or the like. The etchant used substantially etches the sacrificial layer but does not aggressively attack gallium arsenide blocks and/or substrates.

After separating the gallium arsenide blocks from substrate 10, methods of diluting and decanting the wet etchant solution remove the blocks from the solution. In the gallium arsenide example, the wet etchant is diluted and decanted using purified water, methanol, ethanol, or the like. Optionally, a rinsing step occurs after the diluting and decanting step. The rinsing step relies on solutions such as acetone, methanol, ethanol, or any other inert solution having low corrosive properties. Such solution also provides a medium (or fluid) for creating a mixture having blocks suspended therein or generally a slurry.

Instead of the lift-off technique illustrated in Fig. 3, an alternative lift-off method creates intermediate structure 250 of Fig. 4 from the gallium arsenide structure of Fig. 2a. Such alternative lift-off method also promotes lift-off of the shaped blocks in applications where the devices are formed onto the backside of the blocks. As shown, the method includes spreading a filler or wax layer 253 preferably high temperature wax overlying the top surface of exposed portions of sacrificial layer 13 and gaps 255 between each block 19. One such wax includes a product by the name of TECH WAX made by TRANSENE Co., Inc. The method then includes inverting the gallium arsenide structure of Fig. 2a and attaching top surface 21 onto intermediate substrate 257. Such intermediate substrate is, for example, a silicon wafer or the like. However, prior to the attaching step, intermediate substrate surface 261 undergoes steps of etching off any native oxide preferably with a wet etchant such as hydrofluoric acid, and treating the cleaned surface with an adhesion promotor such as hexamethyldisilazane also called HMDS. In removing gallium arsenide substrate 10, backside 263 is lapped until about 50 μm remains on substrate 10. The remaining thickness of substrate 10 is then etched up to aluminum arsenide layer 13. An etchant such as ammonium hydroxide and

hydrogen peroxide (6:200 NH$_3$OH:H$_2$O$_2$) preferentially etches the gallium arsenide substrate up to aluminum arsenide layer 13. Accordingly, the aluminum arsenide layer acts as an etch stop protecting gallium arsenide blocks 19. Removing aluminum arsenide layer 13 requires a step of wet etching using an etchant such as hydrofluoric acid. Such etchant typically removes aluminum arsenide layer 13 after a short dip in such solution. After the aluminum arsenide layer is completely removed, steps including masking, sputtering, and etching form metallized ring contacts 265 as illustrated in Fig. 5. Such metallized ring contacts were made by patterns formed from photoresist layer 267. The metallization for such contacts include materials such as gold, aluminum, among others. Alternatively, other processing steps such as etching, masking, implantation, diffusion, and the like may be performed on the blocks to create other profiles as well as active devices thereon. A solution such as trichloroethane (TCA) dissolves the filler or wax disposed between each block 19 and photoresist layer 21, and lifts off the gallium arsenide blocks 19 from intermediate substrate 257. To decrease corrosion, the gallium arsenide blocks are transferred to an inert solution such as acetone, methanol, ethanol, or any other solution having low corrosive characteristics. Such inert solution and blocks are often called a mixture or generally a slurry.

In another specific embodiment, the method provides as another example steps of forming trapezoidal shaped blocks from a silicon-type wafer as illustrated in Fig. 18. Such steps include providing a second substrate, such as a silicon wafer 700 defining a block layer 703 with a bottom surface 705 and an upper surface 707. In this embodiment, silicon wafer 700 is a single-side-polished wafer having a dimension of about 2" to about 16" with a thickness of about 10 μm to about 2000 μm, and is preferably a two inch silicon wafer of about 235 μm thickness. Bottom surface 705 is the polished side of silicon wafer 700, and upper surface 707 is the unpolished, rough side. The method also includes forming a sacrificial layer 709 overlying upper surface 707 by a technique such as chemical vapor deposition, sputtering, molecular beam epitaxy, or the like. Sacrificial layer 709 is a layer made of silicon nitride (SiN$_x$), silicon dioxide SiO$_2$, metals, or organics, with a thickness of about 100 Å to about 100 μm, and is preferably a SiN$_x$ layer of about 0.4 μm thickness. Similarly to the gallium arsenide block fabrication example, masking and etching steps can be used to form out of block layer 703 the trapezoidal shaped blocks or truncated pyramid shapes. In this embodiment, the trapezoidal shaped block or truncated pyramid shaped structure includes a base with four sides protruding therefrom to a larger top surface. Each side creates an angle between about 20° and about 90° from the top surface to a side, and preferably is about 55°. The block may have a length between about 1 μm and about 1 cm, and a width between about 1 μm and about 1 cm, and preferably has a length of about 1.0 mm and a width of about 1.2

mm. The larger face is on and in contact with sacrificial layer 709. A subsequent step of preferential etching removes sacrificial layer 709 to free each trapezoidal shaped block formed overlying sacrificial layer 709. The blocks are then transferred into a fluid to form a slurry containing the larger trapezoidal shaped blocks.

In yet another specific embodiment, the method provides as another example steps of forming trapezoidal shaped blocks from a silicon-on-insulator (SOI) wafer as illustrated in Fig. 19. Such steps include providing a second substrate such as a SOI wafer 800, that defines a silicon substrate 803 with an upper surface 805, a sacrificial layer 807 overlying upper surface 805, and a block layer 809 overlying sacrificial layer 807. Sacrificial layer 807 composed of SiO_2 is an insulator layer of SOI wafer 800 and block layer 809 composed of silicon is a silicon-on-insulator layer of SOI wafer 800. In this embodiment, SOI wafer 800 has a silicon-on-insulator layer of a thickness of about 1 μm to about 2000 μm, and an insulator layer of thickness of about 100 Å to about 1000 μm, and preferably has a silicon-on-insulator layer of about 35 μm thick silicon, and an insulator layer of about 0.4 μm thick SiO_2. Similarly to the other block fabrication examples, masking and etching steps can be used to form out of block layer 809 the trapezoidal shaped blocks on and in contact with sacrificial layer 807.

In this embodiment, the trapezoidal shaped block or truncated pyramid shaped structure includes a base with four sides protruding therefrom to a larger top surface. Each side creates an angle between about 20° and about 90° from the top surface to a side, and preferably is about 55°. The block may have a length between about 1 μm and about 2000 μm, and a width between about 1 μm and about 2000 μm, and preferably has a length of about 150 μm and a width of about 150μm. As in the silicon example having larger trapezoidal shaped blocks, the larger face of the smaller trapezoidal shaped blocks is in contact with sacrificial layer 807. A subsequent step of preferential etching removes sacrificial layer 807 to free each trapezoidal shaped block formed overlying sacrificial layer 807. Of course, trapezoidal shaped blocks can be removed from contact with the sacrificial layer by steps such as preferential etching, ion milling, or dissolving the sacrificial layer. The blocks are then transferred into a fluid to form a slurry.

In the two preceding examples of forming trapezoidal shaped blocks from silicon, the slowest etching planes for silicon in the $KOH:H_2O$ etching solution used are the {111} planes, which can be considered etch stops forming the sloping sides of the shaped blocks. In each silicon example, the respective mask used to define the blocks must be aligned to the appropriate crystal axis. As shown in Fig. 20, a mask 850 was used to form the silicon trapezoidal blocks 855. Silicon trapezoidal shaped block 855 is formed at the intersection of the diagonal lines on mask 850, and the larger face 860 of silicon trapezoidal shaped block 855 is in contact with

sacrificial layer (respectively 709 and 807, for the first and second preceding silicon examples). The width of the diagonal mask lines in Fig. 20 must be twice the thickness (t) of silicon block layer. For the larger silicon trapezoidal blocks, a = 0.2 mm and silicon block layer 703 has t = 235 μm; whereas, for the smaller silicon trapezoidal blocks, a = 0 and silicon block layer 809 has t = 35 μm.

For each preceding silicon example, etching is completed when silicon block layer 703 or 809 is etched entirely through, and simultaneously when the corners are precisely formed. Continuing etching beyond this point does not change the overall dimensions of the trapezoidal shaped block, but merely rounds the corners. Because of geometric considerations, the width of the top face of the shaped block must be at least $3\sqrt{2}$ times the thickness of the silicon block layer. This limits the aspect ratio of the blocks fabricated by this technique. This mask pattern utilizes as high as 50% of the silicon area if there is no distance between block corners.

In the first silicon example with the larger shaped blocks, the etched silicon wafer is placed in concentrated HF etch solution to remove the shaped blocks from contact with the SiN_x sacrificial layer and any remaining SiN_x from the mask layer. In the second silicon example with the smaller shaped blocks, the etched SOI wafer similarly is placed in concentrated HF etch solution to remove the shaped blocks from contact with the SiO_2 sacrificial layer and any remaining SiN_x from the mask layer. This HF etch solution preferentially etches the SiO_2 and the SiNx to free the shaped blocks without etching the silicon shaped blocks. In particular, a HF solution having a concentration of about 1:1 $HF:H_2O$ was used to etch the sacrificial layer and residual SiNx to free the shaped blocks.

The slurry comprises an inert solution (of fluid) and shaped blocks. Enough solution exists in the slurry to allow the blocks to slide across the top surface of the substrate. Preferably, the amount of solution in the mixture is at least the same order as the amount of blocks. Of course, the amount of solution necessary depends upon characteristics such as block size, block material, substrate size, substrate material, and solution. After preparation, the slurry is transferred or spread over top surface 53 of silicon substrate 50 as illustrated in Fig. 6. The details of the transferring technique are discussed below after a brief discussion in fabricating silicon substrate 50.

As shown in Fig. 6, silicon substrate 50 comprises etched recessed regions 55. A variety of techniques including wet etching, plasma etching, reactive ion etching, ion milling, among others provide recessed regions 50, or generally trenches, receptors, or binding sites. Such techniques etch recessed regions 50 with a geometric profile which is complementary to block 19. In the silicon substrate, for example, each recessed region includes a trapezoidal profile or inverted truncated pyramid shape. The trapezoidal profile allows block 19 to

self-align and fit closely into recessed region 50 via the improved transferring technique.

The transferring technique includes a step of evenly spreading or pouring the slurry over top surface 53. The transferring technique may be accomplished by pouring a vessel of slurry evenly over top surface 53. Alternatively, the slurry may also be transferred from a pipet, flask, beaker, or any other type of vessel and/or apparatus capable of evenly transferring the slurry over top surface 53. Generally, the slurry is poured over top surface 50 at a rate which allows substantial coverage of the top surface, but prevents blocks already disposed into the recessed regions from floating or popping out. Slurry flow is typically laminar but can be non-laminar, depending upon the particular application. In the gallium arsenide block example, the fluid flux over top surface 53 occurs at a velocity between about 0.01 mm/sec. and about 100 mm/sec. Preferably, fluid flux occurs at about 1 mm/sec. At such flux rates, the blocks flow evenly with the fluid, tumble onto top surface 53, self-align, and settle into recessed regions 55. Optionally, to prevent the blocks already disposed in the recessed regions from floating out, the transferring step may take place in a centrifuge or the like. A centrifuge, for example, places a force on the blocks already disposed in the recessed regions and thereby prevents such blocks from floating out with solution.

Alternatively, the transferring technique may be accomplished by a method and related apparatus that includes circulating the slurry over top surface at a rate which allows blocks to dispose into the recessed regions. The rate may be adjusted to permit the blocks to fill the recessed regions so a desired fill-factor is achieved. The slurry is recirculated at a rate so that blocks which are not already disposed continuously flow across top surface until a certain fill-factor is attained. Optimally, the slurry is recirculated at a rate which does not disturb blocks already disposed into recessed regions.

The circulation rate is adjustable to accomodate a desired fill-factor, which will vary depending on the size of the blocks, number of recessed regions, and the specific application. Some applications require the integration of silicon circuits onto transparent substrates such as glass or plastic for use in an active matrix flat panel display. Each pixel or pixel element would have a small corresponding circuit assembled by the method. Larger circuits could also be assembled, such as for multichip modules which might require a number of different larger circuits on the same substrate. Each of these circuits could be etched to a specific shape and assembled by the method into matching recessed regions. Different applications can also require different fill-factors. For example, multichip modules could tolerate lower fill-factors than flat panel displays, because of the difference in number of components. The method and apparatus of the present invention exhibit high fill-factors for different sizes of shaped blocks. After the shaped blocks have been assembled onto the sub-

strate, the disposed blocks can then be bonded and planarized, or the like, if necessary.

In order to continuously flow shaped blocks across the substrate, an apparatus circulates the slurry containing the shaped blocks across the substrate. The shaped blocks and fluid circulate within the apparatus and generally tumble onto the top surface of the substrate which is also contained in the apparatus. The shaped blocks self-align and engage with a recessed region having a complementary shape. The shaped blocks which are not disposed into recessed regions flow off the substrate and enter the recirculation path of the apparatus to flow over the substrate for disposition into recessed regions until a certain fill-factor is achieved.

As illustrated in Fig. 21, an apparatus 900 includes a vessel 903 and a pump 905. In this particular embodiment, apparatus 900 was made entirely of glass but may be constructed of other suitable materials. Vessel 903 includes a receptacle 907 and a conduit 909. Vessel 903 contains a substrate 911 having recessed regions and the mixture of fluid and shaped blocks. Conduit 909, coupled to receptacle 907 which contains substrate 911, includes an input 913, an output 915 leading back to receptacle 907, and a column 917 coupled at one end to input 913 and at the other end to output 915. Pump 905 is coupled to input 913 and dispenses a gas into conduit 909 to facilitate circulation of the fluid and shaped blocks over substrate 911 at a rate where at least one shaped block is disposed into a recessed region.

Receptacle 907 includes a holder 919 and a funneled bottom 921. Holder 919 secures substrate 911 and is capable of moving substrate 911 to facilitate the filling of the recessed regions. Additionally, holder 919 agitates or orients substrate 911 so that shaped blocks not disposed in recessed regions can flow off substrate 911 and back into a recirculation path in vessel 903. The bottom of receptacle 907 is funneled to cause the shaped blocks not disposed into recessed regions on substrate 911 to fall to the bottom of receptacle 907 for recirculation through vessel 903. Shaped blocks not disposed into recessed regions then recirculate through vessel 903.

More specifically, funneled bottom 921 is coupled to input 913 of conduit 909. Shaped blocks not disposed into recessed regions tumble to funneled bottom 921 to input 913 of conduit 909, where pump 905 dispenses a gas, such as nitrogen. The injected gas forms bubbles within the fluid inside column 917 of conduit 909. A gas bubble transports a portion of the fluid and at least one shaped block funneled to input 913 through column 917 back to receptacle 907 through output 915 for attempted disposition into a recessed region. The gas bubble rises through column 917 and transports the fluid and the shaped block to output 915 leading back to receptacle 907.

In this embodiment, apparatus 900 uses nitrogen bubbles to circulate the fluid and the shaped blocks over

substrate 911 without damaging the shaped blocks. Depending on, among other factors, the material of the shaped blocks and the fluid used, apparatus 900 may use other media, or gases such as air, hydrogen (H$_2$), nitrogen (N$_2$), oxygen (O$_2$), or argon (Ar) which do not damage the blocks or otherwise react with the flu at which pump 905 dispenses the gas or transport medium can be changed to achieve different fill-factors of the recessed regions.

In a specific embodiment, the resulting structure 20 of the method described by Figs. 1-3 and 6 is illustrated in Fig. 7. The assembled microstructure includes silicon substrate 10, gallium arsenide blocks 19, and recessed regions 55. The trapezoidal shape of the blocks and recessed regions allows a block to self-align and fit closely into a recessed region during the transferring step. An angle (A) formed between one side of the block and the corresponding side of the recessed region is between about substantially 0° to about 20°. Preferably, such angle is less than about 5° but greater than substantially 0°. Such angle facilitates the self-alignment process of each block. The improved method allows for the fabrication of multiple blocks or microstructures onto a substrate by various shaped blocks and recessed region geometries and the fluid transferring step.

In a modification to the preceding specific embodiment, the blocks 19 are attached into recessed regions 55 through eutectic layer 75 as represented in structure 70 of Fig. 8. Prior to the lift-off step, a metallized layer such as gold, silver, solder, or the like is formed onto surface 73. Alternatively, the layer attaching the block with each recessed region may be a synthetic adhesive or the like instead of a eutectic layer. Process steps comprising masking, etching, and sputtering typically form such metallized layer. Subsequent to the transferring step, heating structure 70 forms eutectic layer 75 between metallization layer 73 and silicon substrate 10. The eutectic layer provides both mechanical and electrical contact between substrate 10 and block 19. The method of attaching the blocks onto the substrate provides an efficient, cost effective, and easy technique.

In an alternative specific embodiment, the portions of the improved method of Figs. 1, 2, 4, 5, and 6 provides the resulting gallium arsenide light emitting diodes (LED) 200 as illustrated in Fig. 9. As shown, the gallium arsenide LED includes silicon substrate 203 and gallium arsenide block 205. Each gallium arsenide block includes at least metallized ring contacts 207, p-type gallium arsenide layer 209, n-type gallium arsenide layer 211, and eutectic layer 213. To illuminate the device, voltage is applied to metallized ring contact 207 or metallization layer. Photons (hv) are illuminated from a center region within each metallized ring contact 207 of gallium arsenide block 205 as shown.

In a further alternative specific embodiment, the improved structure forms gallium arsenide light emitting diodes (LED) 90 as depicted in Fig. 10. Like the previous embodiment, the gallium arsenide LED includes silicon substrate 93 and gallium arsenide block 95. Each

gallium arsenide block also includes at least metallized surface 97, p-type gallium arsenide layer 101, n-type gallium arsenide layer 103, and eutectic layer 105, similar to the preceding embodiment. To illuminate the device, voltage is applied to metallization layer 97 by, for example, a probe. Photons (hv) are illuminated from an edge region instead of a center region of gallium arsenide block 95 as shown.

Still in another specific embodiment, the improved structure forms gallium arsenide structure 120 having tapered aperture opening 123 as illustrated in Fig. 11 (not to scale). A process step such as wet etching, ion milling, reactive ion etching, and others forms the tapered aperture opening 123. The gallium arsenide structure may be an LED, laser, or the like. Similar to the previous embodiment, gallium arsenide structure 120 includes substrate 125 and gallium arsenide block 127. Structure 120 also includes a top metallization layer 131 such as aluminum overlying gallium arsenide block 127 and an insulating layer 133. A ring contact layer 135 provides mechanical and electrical contact between substrate 125 and gallium arsenide block 127. Mechanical support and electrical contact for the gallium arsenide block comes from ledge 137. Also shown is a light emitting (or lasing) aperture 139 having a dimension between about 5 μm and about 40 μm. To turn-on the device, voltage is applied to metallization layer 131. Photons (hv) illuminate from gallium arsenide block 127, through light emitting aperture 139, and through tapered aperture opening 123 as shown. Fiber optic cable 141 receives the photons.

The improved method and resulting structure are in context to a trapezoidal shaped block made of gallium arsenide or silicon merely for illustrative purposes only. Alternatively, the improved method and structure can be in context to almost any block having shaped features. Shaped features allow such blocks to move over the surface of the substrate via fluid transport, align with a corresponding recessed region, and insert into such recessed region. Fig. 12 illustrates further examples of the shaped blocks. As shown, the blocks may, for example, include a rectangular shape 300, octagonal shape 303, or circular shape 305. The rectangular shaped block includes up to four orientations for insertion into a substrate having a corresponding recessed region. Alternatively, the octagonal shaped block includes up to eight orientations and the circular shaped block includes continuous orientations as long as the narrow end inserts first into the recessed region. Such blocks may also comprise a material such as silicon, gallium arsenide, aluminum gallium arsenide, diamond, germanium, other group III-V and II-VI compounds, multilayered structures, among others. Such multilayered structures may include metals, insulators such as silicon dioxide, silicon nitride and the like, and combinations thereof. Generally, the block can be made of almost any type of material capable of forming shaped features. Typically, such blocks are fabricated by methods including ion milling, reactive ion etching, and the

like. In facilitating alignment of each block onto a recessed region, an angle between a side of the block and the corresponding side of the recessed region for a disposed block is between about substantially 0° to about 20°. Preferably, such angle is less than about 5° but greater than substantially 0°.

The shaped block assembles with a substrate such as a silicon wafer, plastic sheet, gallium arsenide wafer, glass substrate, ceramic substrate, or the like. The substrate includes almost any type of material capable of forming shaped recessed regions or generally binding sites or receptors thereon which complement the shaped blocks.

Examples

To prove the principle and demonstrate the operation of the method and structure, a gallium arsenide block in the form of a diode was assembled onto a silicon substrate and operated.

In a gallium arsenide example, a slurry including gallium arsenide blocks were transferred such that the blocks self-aligned into recessed regions located on a top surface of a silicon substrate. The steps for such method included forming the gallium arsenide blocks, transferring the blocks into a solution forming a slurry, and transporting the slurry evenly over a top surface of a silicon substrate having recessed regions. The shaped blocks generally tumble onto the top surface of the substrate, self-align and engage with a recessed region having a complementary shape.

In creating the silicon substrate, a solution of ethylenediamine pyrocatechol pyrazine (EDP) or potassium hydroxide (KOH) produced recessed regions having a trapezoidal profile or inverted truncated pyramid shape. Each solution created trapezoidal shaped profiles having an outward slope of about 55° from an angle normal to the top surface of the substrate. Trapezoidal profiles occurred due to the selectivity (1:100) between the {111} plane and the {100} or {110} plane. Specifically, the {111} plane etched slower than the {100} or {110} plane by a ratio of 1:100.

In the present example, an EDP solution etched recessed regions into a silicon substrate. EDP includes ethylenediamine (about 500 ml.), pyrocatechol (about 160 gms.), water (about 160 gms.), pyrazine (about 1 gm.). The EDP bath was also at a temperature of about 115 °C. Prior to the etching step, a thermal oxide (SiO_2) layer having a thickness of about 200 nm was first formed on a top surface of such substrate. Masking and etching such oxide layer formed rectangular shaped regions. Such regions were then etched vertically about 10 μm forming square openings on the top surface about 23 μm in length. Sides protrude down symmetrically from each opening to a square base having a length of about 9μm.

In fabricating trapezoidal shaped blocks, an epi-ready two inch n-type gallium arsenide wafer provided a substrate for the formation of the self-aligning blocks.

Native oxide on the top surface of such block was first cleared off by a desorption process. The desorption process included exposing the wafer to a temperature of about 700 °C and elements including arsenic. After the desorption step, a sacrificial layer comprising 1 μm of doped or undoped aluminum arsenide was grown on and in contact with the top surface. A thickness of about 10.7 μm of silicon doped gallium arsenide was then grown through an MBE process overlying the aluminum arsenide layer. Silicon dopants were at a concentration of about 10^{18} atoms/cm^3. The top surface of the MBE grown layer was then patterned with photoresist.

Patterning the top surface of the MBE grown layer included spreading a photoresist layer having a thickness of about 1.6 μm over the top surface of the MBE grown gallium arsenide layer. The photoresist used is a product made by Shipley under the name of AZ1400-31. Patterning steps also included at least exposing, developing, and baking the photoresist. Such baking step occurred at a temperature of about 120 °C for about 1 hour to hard-bake the photoresist layer. The patterning steps formed a plurality of rectangles each having a dimension of about 35 μm by 24 μm (exposed portions of the photoresist) on the top surface.

After patterning, unexposed regions were etched forming trapezoidal shaped blocks attached to the aluminum arsenide sacrificial layer. Proper fit between the block and the recessed region requires each block to have substantially the same shape. Accordingly, various concentrations and techniques of wet etching were tested in this particular example.

Generally, wet etching the unexposed regions produced results which depended upon the orientation of the mask edges. If the mask edges were parallel to the [1$\bar{1}$0] direction, wet etching the unexposed regions created outward sloping profiles from the top surface of each block. Alternatively, wet etching unexposed regions where mask edges were parallel to the [110] direction created inward sloping (or reverse mesa) profiles.

Wet etching produced such different profiles (mesa and reverse mesa) because gallium arsenide includes two distinct sets of {111} planes. In a {111} A or {111} gallium plane, each gallium atom on the surface has three arsenide atoms bonded below. For a {111} B or {111} arsenic plane, each arsenide atom on the surface includes three gallium atoms bonded below. Each arsenide atom in the {111} B layer includes a pair of dangling electrons and is therefore exposed. Such dangling electrons are not present in the structure of the {111} A plane. Accordingly, {111} B planes tend to etch faster than {111} A planes, thereby forming blocks having a reverse mesa shape which is generally incompatible with the recessed regions etched on the silicon substrate.

Mask edges parallel to the [110] plane produced more undercutting than the cases where mask edges were parallel to the [1$\bar{1}$0] plane. In the present example, mask edges parallel to the [110] direction produced

about 1.1 μm of horizontal etching per micron of vertical etching near the tops of the blocks. Regions near the base of the blocks produced etches of about 0.4 μm of horizontal etching per micron of vertical etching. Alternatively, mask edges parallel to the [1$\overline{1}$0] plane produced etches of about 0.8 μm of horizontal etching per micron of vertical etching for regions near the top of the blocks, and 0.1 μm of horizontal etching per micron of vertical etch near the bottom of the blocks. The formation of a square region at the base required a longer mask in the [110] direction.

In addition to mask alignment, etchant concentration also affected the shape of each gallium arsenide block. A solution of phosphoric acid, hydrogen peroxide, and water (H_2PO_3:H_2O_2:H_2O) provided a promising etchant for the MBE grown gallium arsenide layer in the present example. Such etchant created three distinct profiles, depending upon the amount of hydrogen peroxide and water added to phosphoric acid. Dilute concentrations of phosphoric acid (1:1:40 H_2PO_3:H_2O_2:H_2O) created a trapezoidal or mesa shaped profile having a 30° angle between the top surface of the block and a corresponding side. Etchant solutions which were less concentrated produced shallower trapezoidal or mesa shaped profiles at angles from about 10° to 20°. Such shallower profiles were probably a result of etching reactions being transport limited in the {111} B planes.

Higher concentrations of phosphoric acid (1:1:20 H_2PO_3:H_2O_2:H_2O and above) created inward sloping (or reverse mesa) profiles limited by the reaction of the {111} B planes. Preferably, a phosphoric acid concentration (1:1:30 H_2PO_4:H_2O_2:H_2O) between the dilute and concentrated solutions provides better profiles for assembly with recessed regions etched on the silicon substrate. Such etchant produced blocks having angles of 55° parallel to the [110] plane and 49° parallel to the [1$\overline{1}$0] plane, and typically etched the MBE grown layer at a rate of about 0.133 μm/minute (or about 133 nm/min). In producing the results described, etchant solution was typically replenished when depleted.

Increasing the ratio of phosphoric acid to hydrogen peroxide by 3:1 produced similar profiles to the experiments described, but generally caused rough surfaces on the sides. Such rough surfaces were desirable for the present application.

In a modification to this example, a similar wet etchant (1:1:30 H_2PO_3:H_2O_2:H_2O) facilitated the formation of aluminum gallium arsenide blocks from an aluminum gallium arsenide MBE grown layer. Such etchant provided an inward sloping profile parallel to the [110] direction for an aluminum gallium arsenide (x=0.1, Al_xGa$_{l-x}$As) grown MBE layer. Vertical etch rates were about the same as the gallium arsenide MBE grown layer. However, the presence of aluminum arsenide increased etching of the {111} B plane into the reaction-rate limited regime. Such etchant produced an inward sloping profile because etching x=0.1, Al_xGa$_{l-x}$As was more reactive in the {111} B plane than gallium arsenide.

In addition to wet etching, ion milling was also used to create the gallium arsenide trapezoidal shaped blocks. Ion milling the MBE grown gallium arsenide layer provided outward sloping profiles ranging at angles of about 68° to 90° between the top surface and a corresponding side. To produce such angles, the ion beam angles ranged from about 0° to 25° in reference to a normal from the top surface of the MBE grown layer. Steeper beam angles (closer to 90°) generally created vertical or substantially vertical profiles. Ion milling also required the substrate to be rotated about a center axis during such processing step. Other processing variables included an argon gas etchant, pressure of about 50 millitorr, ion energy of about 1000 v, and an ion milling rate of 1 μm every seven minutes. As the photoresist mask eroded laterally about 5 μm every 70 minutes during milling, sidewalls having angles at about 68° were produced. Selectivity between the gallium arsenide and photoresist was about 3:1. Ion milling produced substantially consistent gallium arsenide blocks and was therefore more effective than wet etching in this particular example.

A final bath having a concentration of 1:1:30 H_2PO_3:H_2O_2:H_2O was used to clear off remaining oxides of either gallium arsenide and aluminum arsenide. Such oxides were typically formed when aluminum arsenide was exposed to etching baths or ion milling. Hydrofluoric acid may then be used to clear off the oxide layers (typically rough looking and brown in appearance). Generally, such oxide layers reduce the effectiveness of hydrofluoric acid (HF) etching on the sacrificial aluminum arsenide layer.

After clearing off any oxide layers, a HF solution preferentially etched the sacrificial layer of aluminum arsenide to lift-off the gallium arsenide blocks. In particular, a HF solution having a concentration of about 5:1 H_2O:HF was used to etch the sacrificial layer and lift off the blocks. Any blocks still remaining on the substrate possibly through surface tension can be mechanically removed from the substrate into a solution. Removed blocks include a base dimension of about 22 μm by 23 μm, compared to a designed dimension of 24 μm by 24 μm.

After removing the blocks from the substrate, a teflon pipet was used to remove a substantial portion of the HF solution from the gallium arsenide blocks. Any remaining HF was rinsed off with water. Such rinsing step created a mixture including blocks and water. An inert solution such as acetone then replaced the water to decrease any oxide formation on the blocks. Once in the inert solution, the blocks may cluster together and either float to the surface or settle to the bottom of the solution. Such clusters, often visible to the naked eye, decreased the effectiveness of a subsequent transferring step, and were therefore separated by mechanically agitating the solution with ultrasonic vibration.

The inert solution including gallium arsenide blocks was then transferred (or poured) evenly over the top

surface of the silicon substrate. In particular, a pipet was used to transfer such solution over the top surface of the substrate. The solution is transferred at a rate creating substantially a laminar flow. Such laminar flow allowed the blocks to tumble and/or slide onto the top surface of the substrate and then self-align into the recessed regions via the trapezoidal profile. Generally, the transfer rate should provide an even flow of solution including blocks over the substrate surface but should not free or remove any blocks already disposed into the recessed regions.

Blocks fabricated by ion milling produced higher yields than wet etched blocks. Ion milled blocks having substantially consistent profiles self aligned and inserted into more than 90% of the recessed regions located on the substrate surface before the solution substantially evaporated. As the solution evaporates, surface tension often pulled a portion of the blocks out of the recessed regions. About 30% to 70% of the recessed regions remained filled after evaporation. The decrease in yield can be addressed by using liquids having lower surface tension during evaporation or by super critical drying methods which substantially eliminates surface, tension. Alternatively, blocks may be bonded into the recessed regions prior to evaporation of the solution, thereby fixing the yield. Wet etched blocks having less consistent block profiles inserted correctly into about 1% to 5% of available recessed regions. Accordingly, ion milled blocks provided higher yields relative to the blocks fabricated by wet etching.

Photographs shown in Fig. 13 illustrate gallium arsenide blocks disposed into recessed regions of the silicon substrate 150 according to the present example. A top portion 153 of each recessed region is square and measures about 23 μm at length. As shown, the photograph includes recessed regions 155, silicon substrate 157, and trapezoidal shaped block 159.

To further illustrate the operation of the present example, an illuminated diode 170 is shown in the photograph of Fig. 14. The photograph includes silicon substrate 173 and illuminated gallium arsenide LED 175. The gallium arsenide LED emitted infrared radiation while under electrical bias. Each gallium arsenide LED which was grown on an MBE layer included an N+ gallium arsenide cap layer (about 100 nm thickness), an N+ $Al_{0.1}Ga_{0.9}As$ transport layer (about 1 μm thickness), a P- active region (about 1 μm thickness), and a P+ buffer layer (about 1 μm thickness). The gallium arsenide LED also required a ring metallized contact 400 for applying voltage and an opening 403 for light output at a top portion of each block as illustrated in Fig. 15. A current-voltage (I-V) curve 500 illustrated in Fig. 16 exhibits typical p-n junction characteristics for the gallium arsenide structure of Fig. 14.

Gallium arsenide/aluminum arsenide resonant-tunneling diodes (RTD's) were also integrated onto silicon. RTD's grown on an MBE layer include gallium arsenide wells (depth at about 5.0 nm) between two aluminum arsenide barriers (depth at about 2.5 nm). Current-volt-

age characteristics 600 for the RTD's integrated with silicon exhibited proper differential negative resistance (NDR) at V_{PEAK} = 2.0 v. as illustrated in Fig. 17. At such voltage, peak-to-valley ratio was about 2.5. Oscillations (rf) observed after biasing the RTD's in the NDR region were limited to about 100 MHz. External capacitances and inductances of the biasing circuit caused such limitations in frequency.

The description above is in terms of assembling a gallium arsenide block onto a silicon substrate for illustrative purposes only. As shown, the invention may be applied to forming gallium arsenide diodes onto silicon substrates. Another commercial application includes gallium arsenide lasers assembled with silicon integrated circuits. The silicon chips can communicate with other chips with integrated optical detectors on extremely high bit-rate optical channels. Other applications may also include integration of microwave gallium arsenide devices onto silicon integrated circuits for the purpose of microwave electronics. Still a further application includes microstructures integral with a plastic sheet forming active liquid crystal displays (ALCD) and the like. In such application, the plastic sheet may be fabricated by a technique including stamping, injection molding, among others. Advantages of the invention include for example the applicability of conventional metallization or other processes over the planar surface for interconnection of the integrated electronic devices or portions of electronic devices between the blocks and/or between blocks and other electronic devices on the substrate. The concept of the invention can be used with almost any type of microstructure which assembles onto a larger substrate.

To demonstrate the general operation and effectiveness of the method and apparatus for various applications such as those requiring different sizes of shaped blocks, further examples of the invention involved assembling microstructures on a silicon substrate using shaped trapezoidal blocks of silicon having two different sizes and differing by 2.5 orders of magnitude in mass.

In the first silicon experiment, larger trapezoidal blocks were designed to have two-fold rotational symmetry with the size of the larger face having a dimension of about 1.0 mm x 1.2 mm and a depth of about 235 μm, and recessed regions were designed to correspond to the dimensions of the larger trapezoidal blocks. In the second silicon experiment, smaller trapezoidal blocks were designed to have four-fold symmetry with the size of the larger face having a dimension of about 150 μm x 150 μm and a depth of about 35 μm, and recessed regions were designed to correspond to the dimensions of the smaller trapezoidal blocks. In both experiments, the method and apparatus exhibited high fill-factors.

In each of the silicon examples, the mixture or slurry including silicon shaped blocks and an inert fluid are transported over a top surface of a silicon substrate having complementary recessed regions by use of an apparatus that circulates the slurry over the substrate.

In creating silicon substrates having recessed

regions for, each silicon experiment, a solution of potassium hydroxide (KOH) produced recessed regions having a trapezoidal profile or inverted truncated pyramid shape. The solution created trapezoidal shaped profiles or inverted truncated pyramid shapes having a larger face with lateral dimensions at the top surface with sides sloping inward at about 55° from the top surface of the substrate. Trapezoidal profiles occurred due to the selectivity (1:200) between the {111} plane and the {100} plane. Specifically, the {111} plane etched slower than the {100} plane by the approximate ratio of 1:200.

In the silicon examples, the KOH solution etched trapezoidal recessed regions into about 500 μm thick silicon wafers (5 cm x 5 cm in overall area) using a mask consisting of rectangular openings. The KOH etchant solution used in the examples was a 1:2 (by weight) $KOH:H_2O$ solution at about 80°C. Prior to the etching step, a silicon nitride (SiN_x) mask layer was first formed on a top surface of such substrates.

Masking and etching such silicon nitride layer formed trapezoidal shaped recessed regions. The depth of the trapezoidal recessed region is determined by the length of time the silicon substrate is etched. If the silicon is etched the correct length of time, recessed regions can be made which are identical in shape and size to the blocks.

For the first silicon experiment, the larger recessed regions in the substrate had lateral dimensions of about 1.0 mm x 1.2 mm at the top surface and a depth of about 235 μm after about 23 minutes of etching to complement the larger trapezoidal shaped blocks. In total, the mask in this experiment consisted of 191 holes corresponding to recessed regions, arranged in various test patterns.

For the second silicon experiment, the smaller recessed regions in another substrate had lateral dimensions of about 150 μm x 150 μm at the top surface and a depth of about 35 μm after about 30 minutes of etching to complement the smaller trapezoidal shaped blocks. The mask in this experiment was simply an array of 64 x 64 holes (corresponding to 4,096 recessed regions) with about a 300 μm spacing between consecutive holes.

In the substrates for both silicon experiments, the silicon nitride mask layer was not removed from the substrates and remained on the substrates throughout the microstructure assembling method.

In fabricating the larger trapezoidal shaped blocks for the first silicon experiment, a single-side-polished two inch silicon wafer of about 235 μm thickness provided a substrate for the formation of self-aligning shaped blocks. In this experiment, the silicon wafer itself is the block layer from which the trapezoidal shaped blocks are formed. A SiN_x layer of thickness about 0.4 μm was deposited on both the polished bottom surface of the wafer and the unpolished upper surface of the wafer. The SiN_x layer overlying the unpolished upper surface of the wafer forms a sacrificial layer, and the SiN_x layer overlying the polished bottom surface of the wafer forms a mask layer. The SiN_x mask layer overlying the polished bottom surface of the wafer was then patterned with photoresist.

Patterning the SiN_x mask layer overlying the polished bottom surface of the wafer included spreading a photoresist layer over this SiN_x layer. Patterning steps also included at least exposing, developing, and baking the photoresist. Such baking step occurred at a temperature of about 120°C for about 20 minutes to hard-bake the photoresist layer. The patterning steps formed a plurality of squares (or rectangles). After patterning, exposed regions were etched forming trapezoidal shaped blocks attached to the SiN_x sacrificial layer.

In fabricating smaller trapezoidal shaped blocks for the second silicon experiment, a SOI wafer provided a substrate for the formation of self-aligning shaped blocks. The particular SOI wafer used had a SOI layer of about 35 μm thickness with a silicon dioxide (SiO_2) layer of about 0.4 μm thickness separating it from the rest of the wafer. The 35 μm SOI layer is the block layer of silicon from which the trapezoidal shaped blocks are formed. The SiO_2 layer of about 0.4 μm thickness is the sacrificial layer. A SiN_x mask layer of thickness about 0.4 μm was deposited on both 35 μm silicon block layer and patterned with photoresist.

Patterning the SiN_x mask layer overlying the upper surface of the wafer included spreading a photoresist layer over this SiN_x mask layer. Patterning steps also included at least exposing, developing, and baking the photoresist. The patterning steps formed a plurality of rectangles each having a dimension of about 150 μm x 150 μm (exposed portions of the photoresist). After patterning, unexposed regions were etched forming trapezoidal shaped blocks attached to the SiO_2 sacrificial layer.

The slowest etching planes for silicon in this $KOH:H_2O$ etching solution are the {111} planes, which can be considered etch stops forming the sloping sides of the shaped blocks. In each silicon experiment, the respective mask used to define the blocks must be aligned to the appropriate crystal axis. As shown in Fig. 100, a mask was used to form silicon trapezoidal shaped blocks. Trapezoidal shaped block is formed at the intersection of the diagonal lines on the mask. The width of the diagonal lines in the figure must be twice the thickness of the silicon block layer. For the larger trapezoidal blocks, a = 0.2 mm and t = 235 μm; whereas, for the smaller trapezoidal blocks, a = 0 and t = 35 μm.

Etching is completed when this silicon block layer is etched entirely through, and simultaneously when the corners are precisely formed. Continuing etching beyond this point does not change the overall dimensions of the trapezoidal shaped block, but merely rounds the corners. Because of geometric considerations, the width of the top face of the shaped block must be at least 3√2 times the thickness of the silicon block layer. This limits the aspect ratio of the blocks fabricated by this technique. This mask pattern utilizes as high as

50% of the silicon area if there is no distance between block corners.

In the first silicon experiment with the larger shaped blocks, the etched silicon wafer is placed in concentrated HF etch solution to remove the shaped blocks from contact with the SiN_x sacrificial layer and any remaining SiN_x from the mask layer. In the second silicon experiment with the smaller shaped blocks, the etched SOI wafer similarly is placed in concentrated HF etch solution to remove the shaped blocks from contact with the SiO_2 sacrificial layer and any remaining SiN_x from the mask layer. This HF etch solution preferentially etches the SiO_2 and the SiN_x to free the shaped blocks without etching the silicon shaped blocks. In particular, a HF solution having a concentration of about 1:1 $HF:H_2O$ was used to etch the sacrificial layer and residual SiN_x to free the shaped blocks.

Once all the shaped blocks were free in the solution, the HF was decanted and water was added. For the first silicon experiment, water and the larger shaped blocks formed the mixture or slurry. However, for the second silicon experiment, methanol and the smaller shaped blocks formed the mixture or slurry. As silicon is hydrophobic in nature, smaller shaped blocks having smaller mass tended to float on the surface of the water. The larger blocks did not have this problem because of their larger mass. Since methanol has both polar and nonpolar properties, the smaller shaped blocks did not float but preferably submerged into the fluid. As the silicon examples demonstrate, the selection of the fluid used in the slurry may depend on the mass of the shaped block, among other factors.

In the first silicon experiment, the mixture including approximately 500 of the larger shaped blocks and water (about 0.5 liter) was placed into the apparatus (about 4" diameter). The substrate was about 5 cm x 5 cm and contained 191 recessed regions in various patterns. Initially, small bubbles tended to stick to the larger shaped blocks and to the recessed regions on the substrate, due to the fact that all the silicon surfaces are hydrophobic. Adding a small amount of surfactant of about 5 drops to the water (1:100,000) made the silicon surfaces less hydrophobic and bubbles no longer stuck to the shaped blocks or to the recessed regions. The substrate was oriented at an angle which caused the incorrectly oriented blocks to slide off. Agitation and correct orientation of the substrate increased the rate at which the blocks filled the holes. Because of the tapered shape of the trapezoidal blocks, nearly all the blocks descended through the fluid with the larger surface facing upward. Upon landing on the substrate, the blocks were thus properly oriented to fill the recessed regions, resulting in enhanced fill rates. On repeated runs of this first silicon experiment, all 191 recessed regions were filled for a fill-factor of 100% in about 4.5 minutes.

In the second silicon experiment, the mixture including approximately 30,000 of the smaller shaped blocks and methanol (about 0.5 liter) was placed into the apparatus. The substrate was about 5 cm x 5 cm and contained a 3 cm x 3 cm array of 64 x 64 (4,096) recessed regions in the center of the substrate. Operating the apparatus in a manner similar to that used for the first silicon experiment with the larger shaped blocks resulted in a saturated fill-factor of about 70% after about 15 minutes.

When the larger faces of the shaped blocks are rough, higher fill-factors were achieved. For shaped blocks having smooth larger faces, the shaped blocks tended to stick to the smooth surface of the substrate and reduce the overall motion of the blocks on the substrate, with the fluid flow being insufficient to free blocks stuck in this manner. In the first silicon experiment, the larger shaped blocks did not have this problem since the larger face of the blocks was the rough back of the unpolished wafer. Shaped blocks having features, such as circuits or contact pads, on the larger face have such rough surfaces for higher fill-factors.

Roughening the top surface of the substrate having the recessed regions also leads to higher fill-factors. After removing the SiN_x mask layer, the substrate was lapped in about 0.5 μm Al_2O_3 lapping powder just long enough (about 1-2 minutes) to create about a 0.3 μm roughness on the surface. Blocks in all orientations easily came off the substrate after it was roughened. Using a lapped substrate in the second silicon experiment with smaller shaped blocks, saturated fill-factors of about 90% were achieved after about 15 minutes in the apparatus. After repeated runs of the second silicon experiment, it was determined that the 90% fill-factor achieved for the smaller blocks was a steady state condition.

In order to achieve even higher fill-factors, especially for the smaller shaped blocks, care must be taken to properly etch the substrate and to keep the substrate and solution free of particles that could interfere with filling. For example, interference with filling could occur if the bottoms of the recessed regions are left rough by the KOH etching, or if particulates are deposited inside the recessed regions during the lapping process. Nonuniformity in the bottoms of the recessed regions could either prevent blocks from entering the recessed regions, or aid in the unfilling of the blocks from these recessed regions. Additionally, substrates with recessed regions that were not etched deep enough did not achieve high fill-factors, since the blocks protruding above the edge of the recessed region in the substrate could more easily be removed by fluid flow. Substrates with recessed regions that were etched too deeply also did not achieve high fill-factors. While the lateral dimensions at the top of an overetched recessed region remain the same, the lateral dimensions at the bottom of the recessed region become smaller as the depth is increased. Therefore, only the edges and not the smaller bottom face of a block filling an overetched recessed region will touch the substrate. Optimally, higher fill-factors are achieved when the recessed regions are neither underetched nor overetched.

Also described in general terms is the unique profiles for creating self-assembling devices. Such unique

profiles, for example, are terms of a single block structure having a corresponding recessed region structure on a substrate for illustrative purposes only. The block structure may also include a variety of shapes such as a cylindrical shape, rectangular shape, square shape, hexagonal shape, pyramid shape, T-shape, kidney shape, and others. The block structure includes widths, lengths, and heights to promote self-assembly for a desired orientation. In addition, more than one type of structure may be present in the mixture (solution and blocks) as long as each structure includes a specific binding site on the substrate.

Although the foregoing invention has been described in some detail by way of illustration and example, for purposes of clarity of understanding, it will be obvious that certain changes and modifications may be practiced within the scope of the appended claims.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. Merely by way of example the invention may used to assemble gallium arsenide devices onto a silicon substrate as well as other applications. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

Claims

1. A method of assembling a microstructure on a substrate, said substrate comprising a top surface with at least one recessed region thereon, comprising the steps of:

   providing a plurality of shaped blocks in a fluid to form a slurry; and
   circulating said slurry over said substrate at a rate where at least one of said shaped blocks is disposed at a selected orientation into said recessed region, each of said shaped blocks comprising a tapered edge to fit into said recessed region at said selected orientation.

2. The method of claim 1 wherein each of said shaped blocks includes at least one electronic device.

3. The method of claim 1 wherein each of said shaped blocks includes a portion of an electronic device.

4. The method of claim 1 wherein said substrate is selected from a group consisting of a silicon wafer, plastic sheet, gallium arsenide wafer, glass substrate, and ceramic substrate.

5. The method of claim 1 wherein said fluid is an inert fluid selected from a group consisting of water, acetone, and alcohol.

6. The method of claim 1 wherein said each of said shaped blocks include a trapezoidal profile.

7. The method of claim 6 wherein each of said recessed regions in said substrate is shaped substantially trapezoidal to complement each of said shaped blocks.

8. The method of claim 1 wherein a gas circulates said slurry over said substrate.

9. The method of claim 8 wherein said gas includes nitrogen.

10. The method of claim 1 wherein each of said blocks comprises a semiconductor material.

11. The method of claim 1 wherein each of said blocks comprises a truncated pyramid shape, said truncated pyramid shape including a base and sides protruding from said base to a top.

12. The method of claim 11 wherein said base is rectangular and said sides include four sides.

13. The method of claim 11 wherein said base is square and said sides include four sides.

14. The method of claim 12 or 13 wherein each of said blocks includes a length ranging from about 5 microns to about 2,000 microns, a width ranging from about 5 microns to about 2,000 microns, and a thickness from said base to said top ranging from about 2 microns to about 500 microns.

15. The method of claim 1 wherein a pump recirculates said slurry over said substrate.

16. The method of claim 1 wherein a mechanical means is used to move said slurry over said substrate.

17. A method of transporting a micromachined block comprising an integrated circuit portion, said method comprising:

   placing at least one block in a fluid; and transporting said block to a selected location.

18. The method of claim 17 wherein a pump transports said block.

19. The method of claim 17 wherein a bubble pump transports said block.

20. The method of claim 17 wherein a jet pump transports said block.

21. The method of claim 17 wherein said block self-

aligns into a recessed region of a substrate.

22. The method of claim 17 wherein said block is an etched block.

23. The method of claim 17 wherein a mechanical means is used to move said block and said fluid.

24. A method of forming a hybrid integrated circuit comprising steps of:

    providing a first tapered shaped block including a first electronic device portion thereon, and a second electronic device portion;
    placing said first tapered shaped block into a first recessed region of a substrate; and
    interconnecting said first tapered shaped block with said second electronic device portion, said interconnecting step being a metallization step.

25. The method of claim 24 wherein said second electronic device portion is located on said substrate.

26. The method of claim 24 wherein said second electronic device portion is located on a second tapered shaped block placed into a second recessed region of said substrate.

27. The method of claim 26 wherein a third electronic device portion located on said substrate is interconnected to said first electronic device portion or to said second electronic device portion.
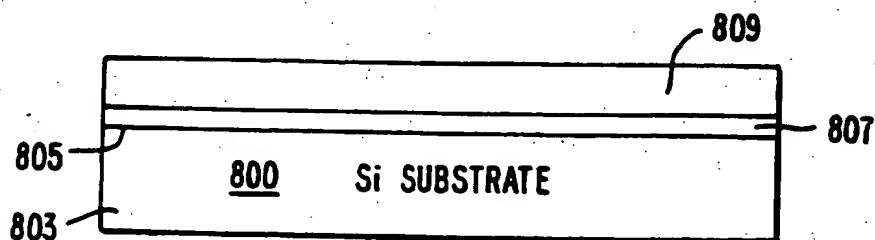
FIG. 1.

FIG. 2A.

FIG. 3.

FIG. 2B.

250

263

GaAs SUBSTRATE   10

13

19   19   19

253

255   21   255   21   261   255   21   255

INTERMEDIATE SUBSTRATE

257

FIG. 4.

267   267   267   267   265   267   267   267

19   19   19

INTERMEDIATE SUBSTRATE   257

FIG. 5.

19   19   19

19

19   19   GaAs
BLOCK
19

53
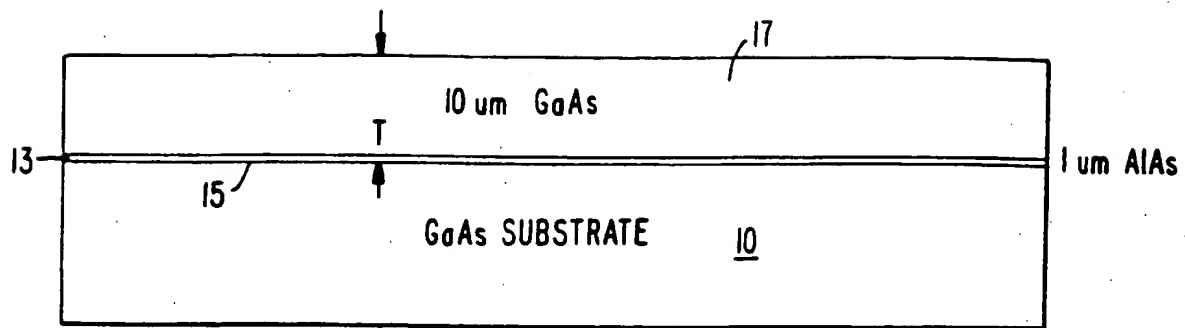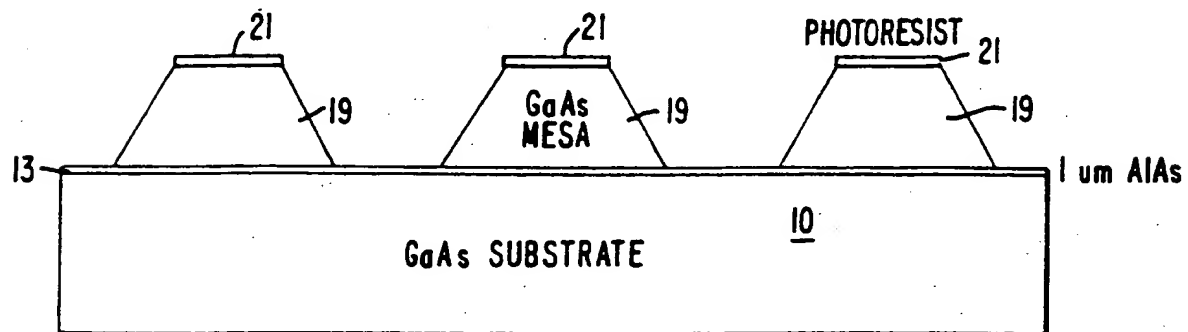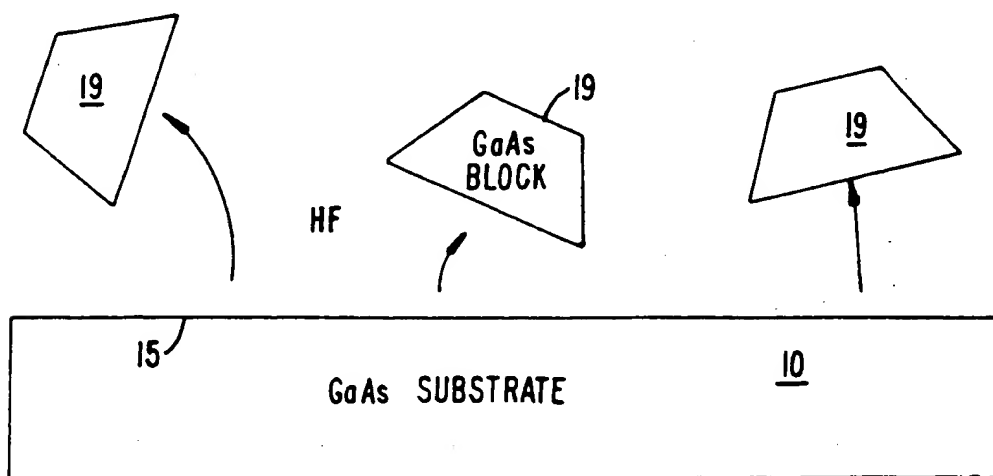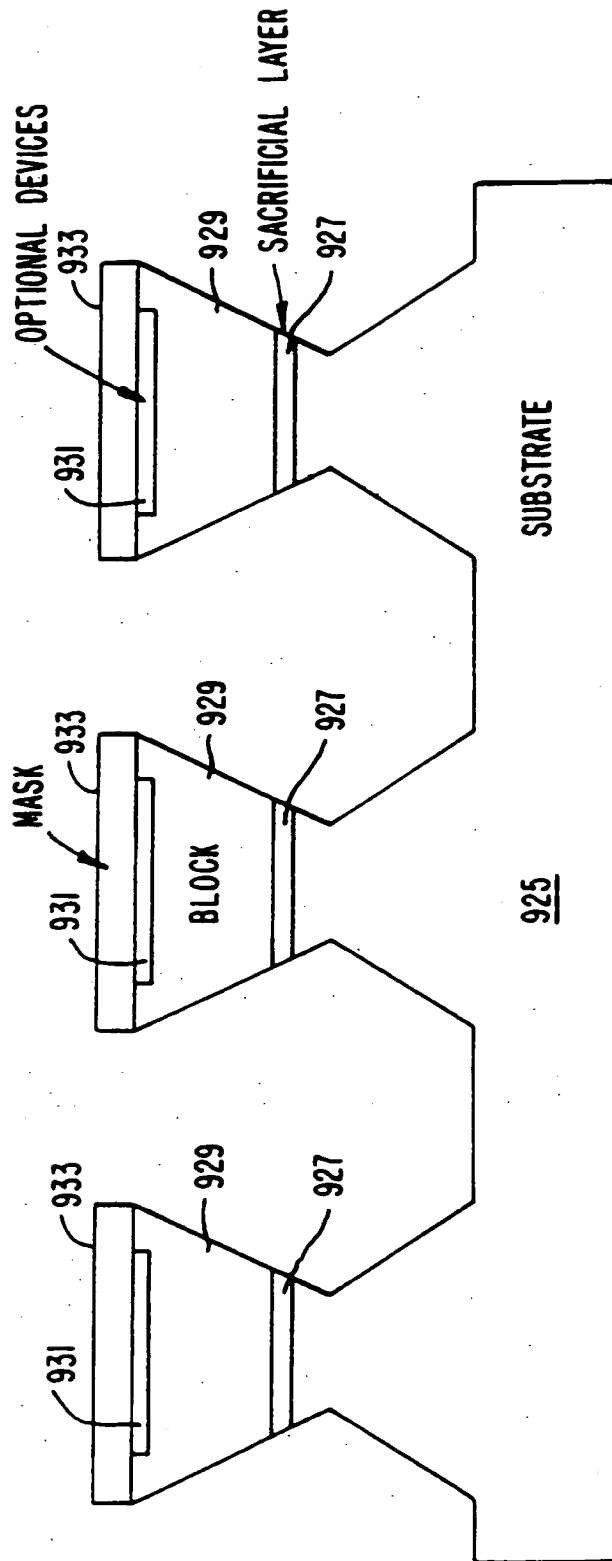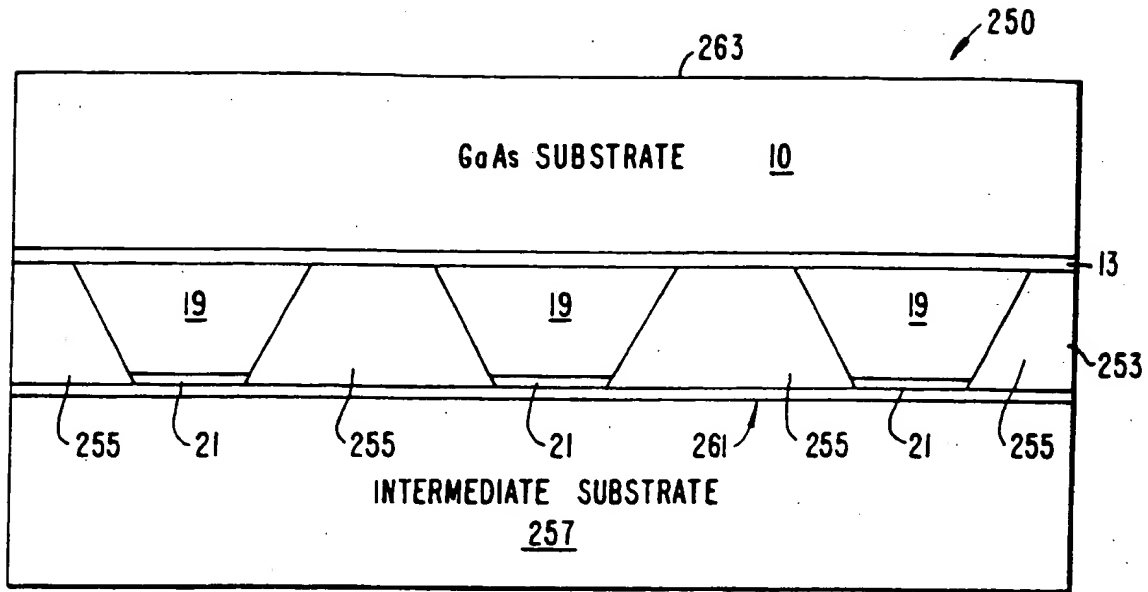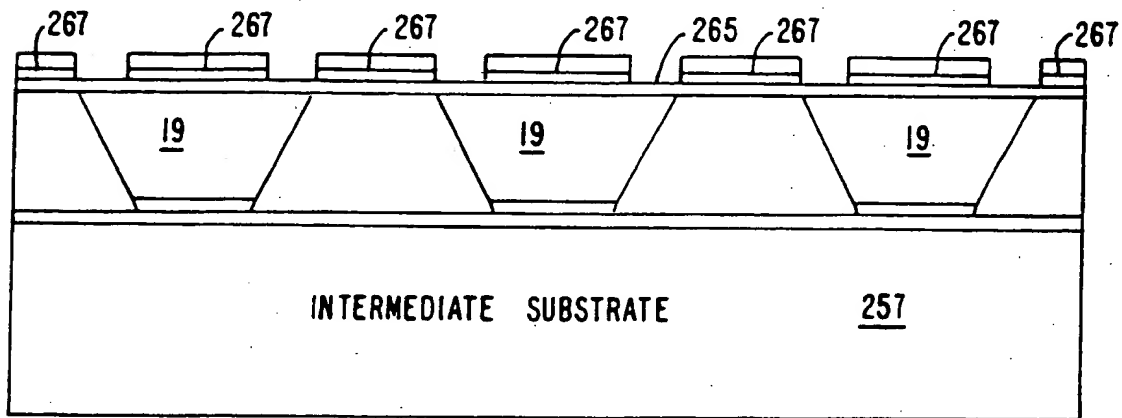
55   55 Si SUBSTRATE   50   55
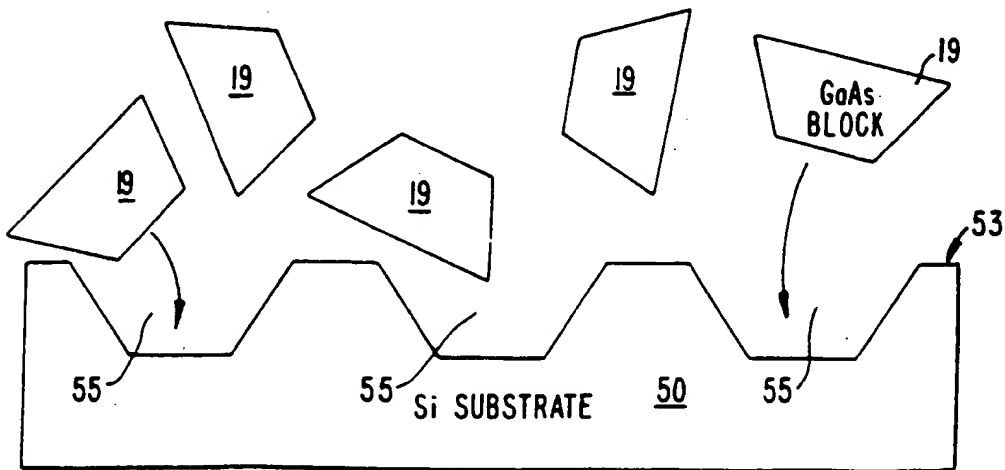
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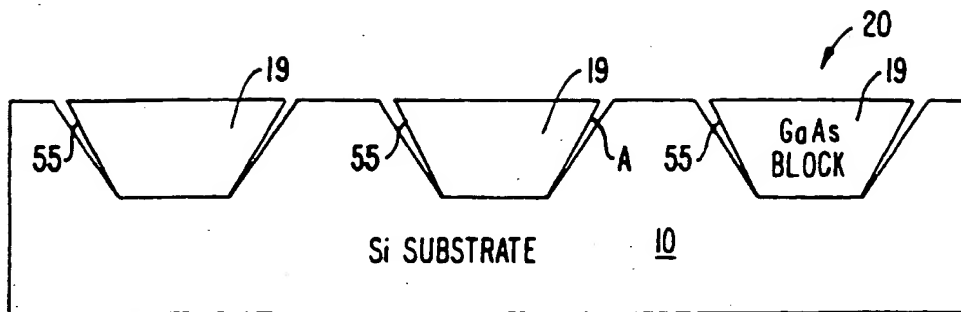
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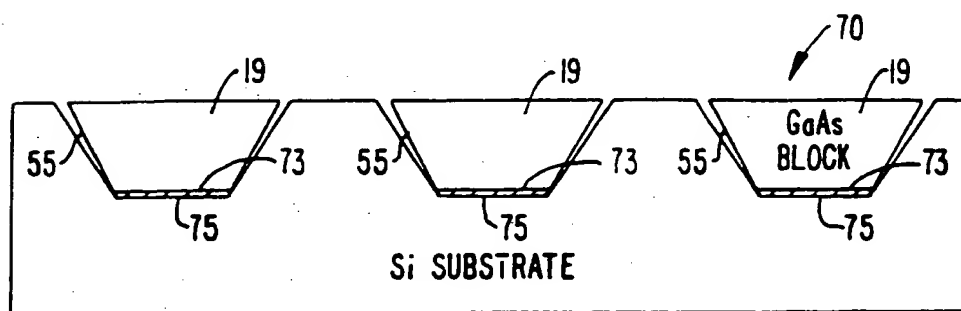
FIG. 8.

FIG. 9.

FIG. 10.

FIG. II.

FIG. 12.

FIG.13

FIG.14
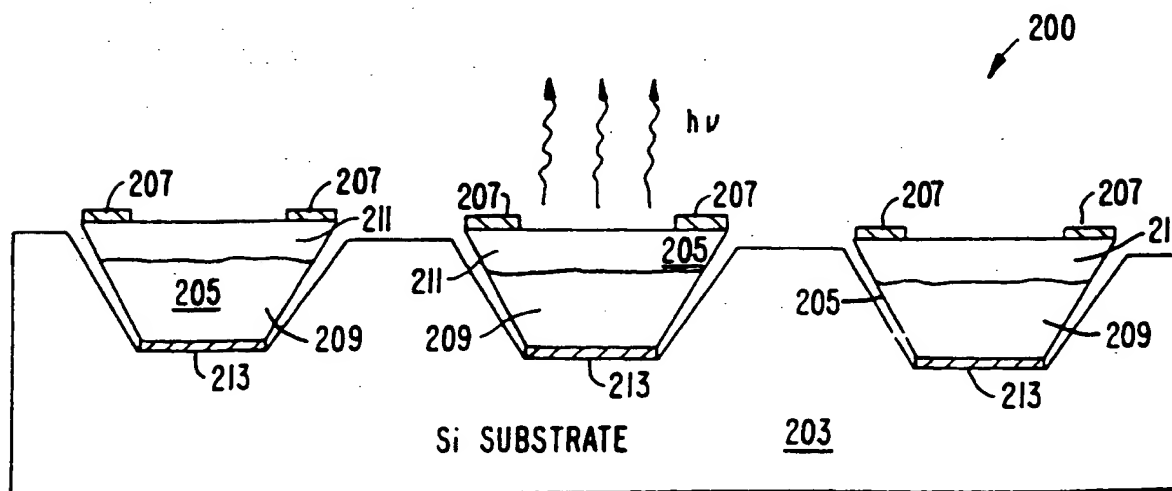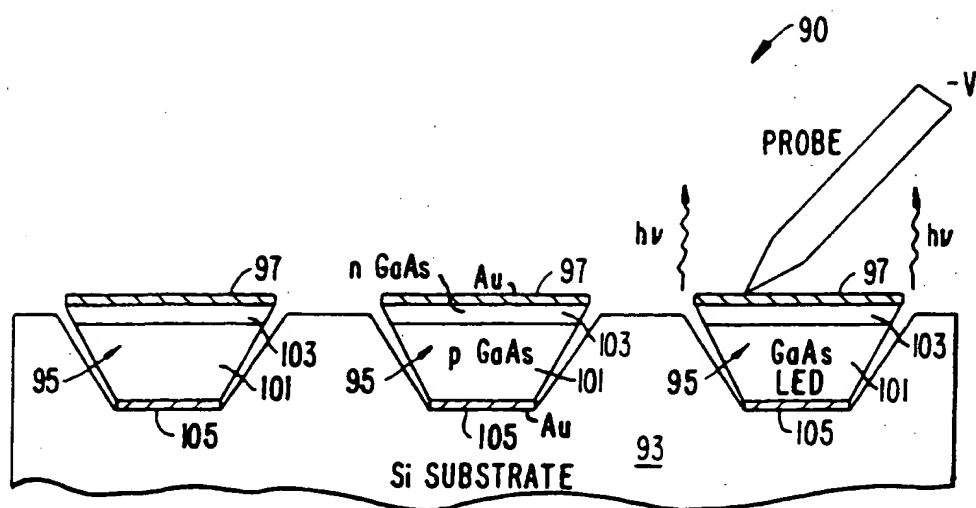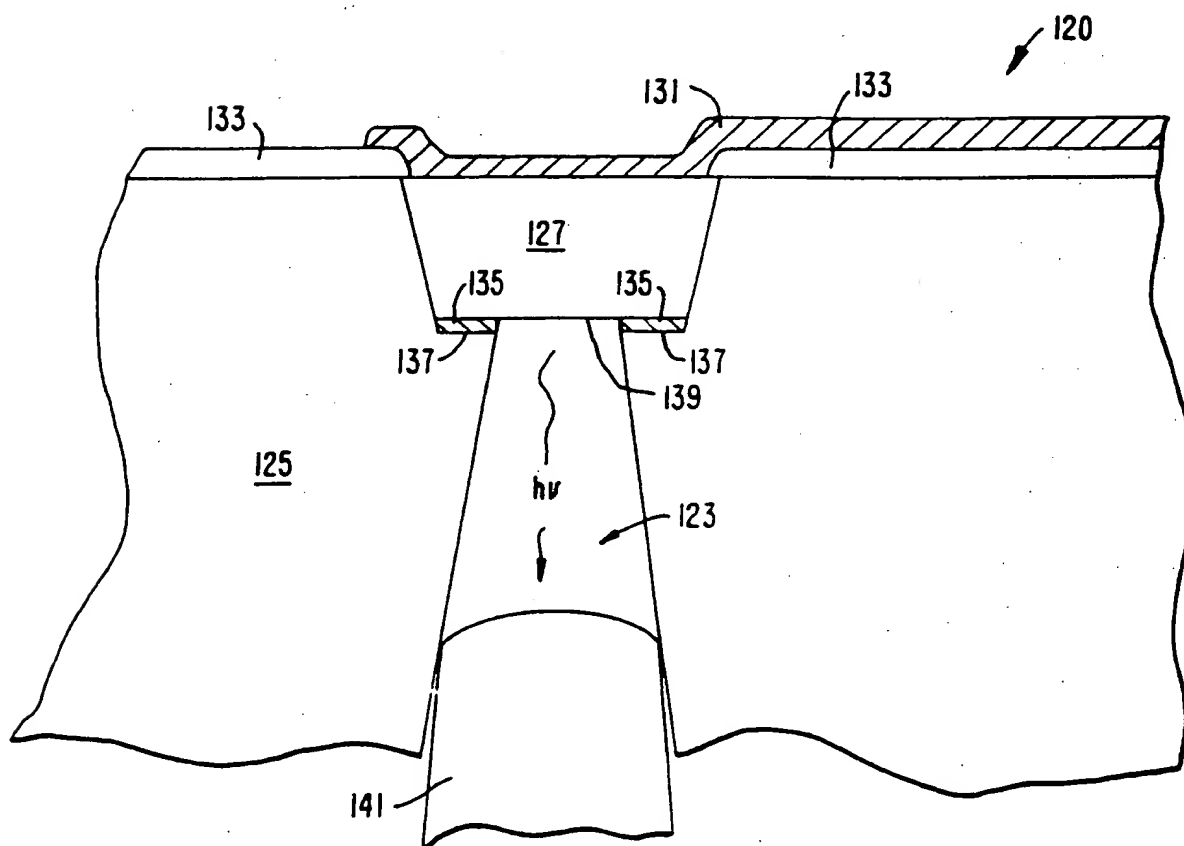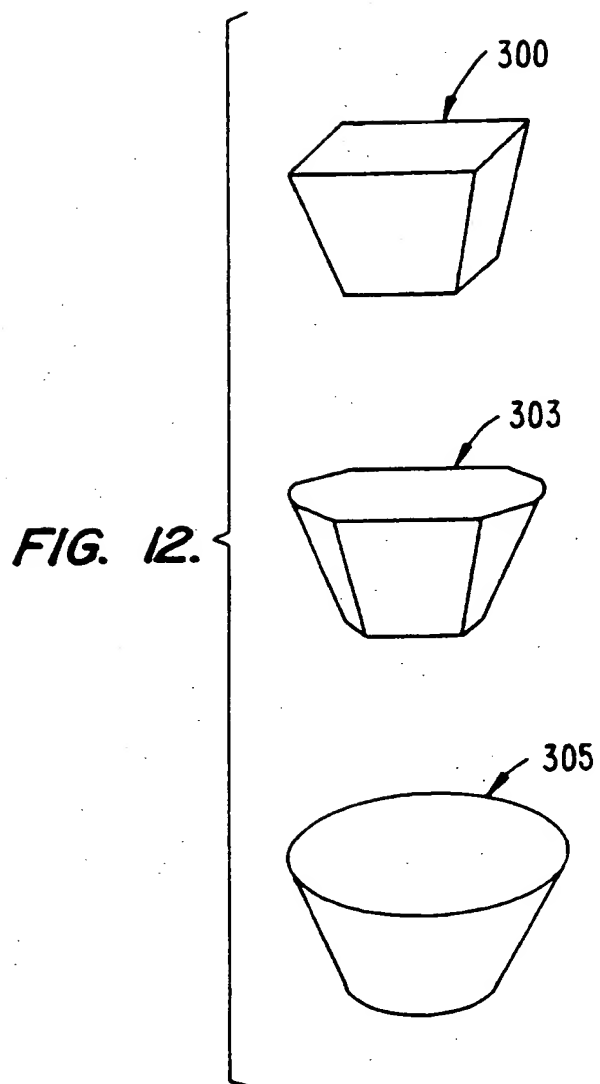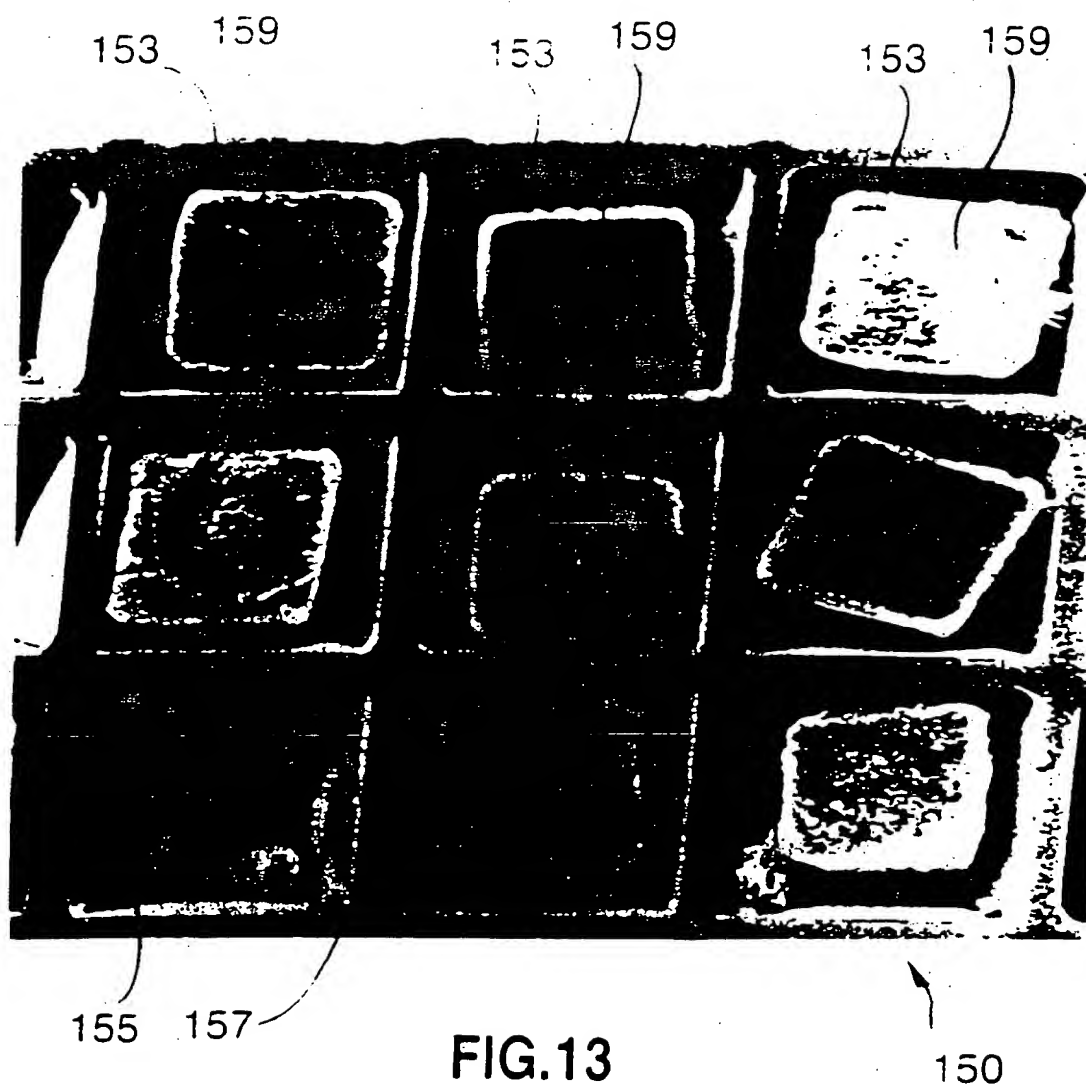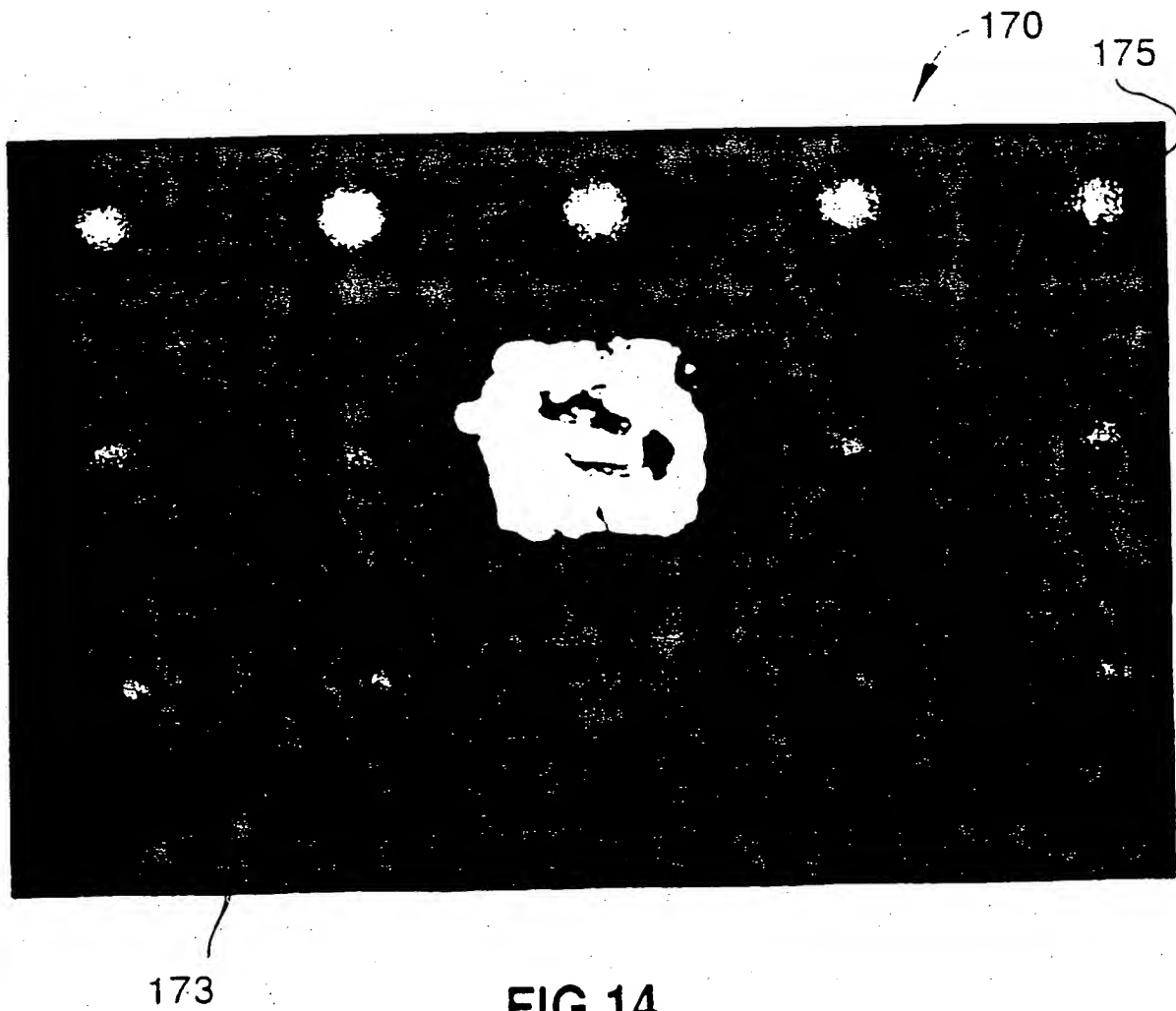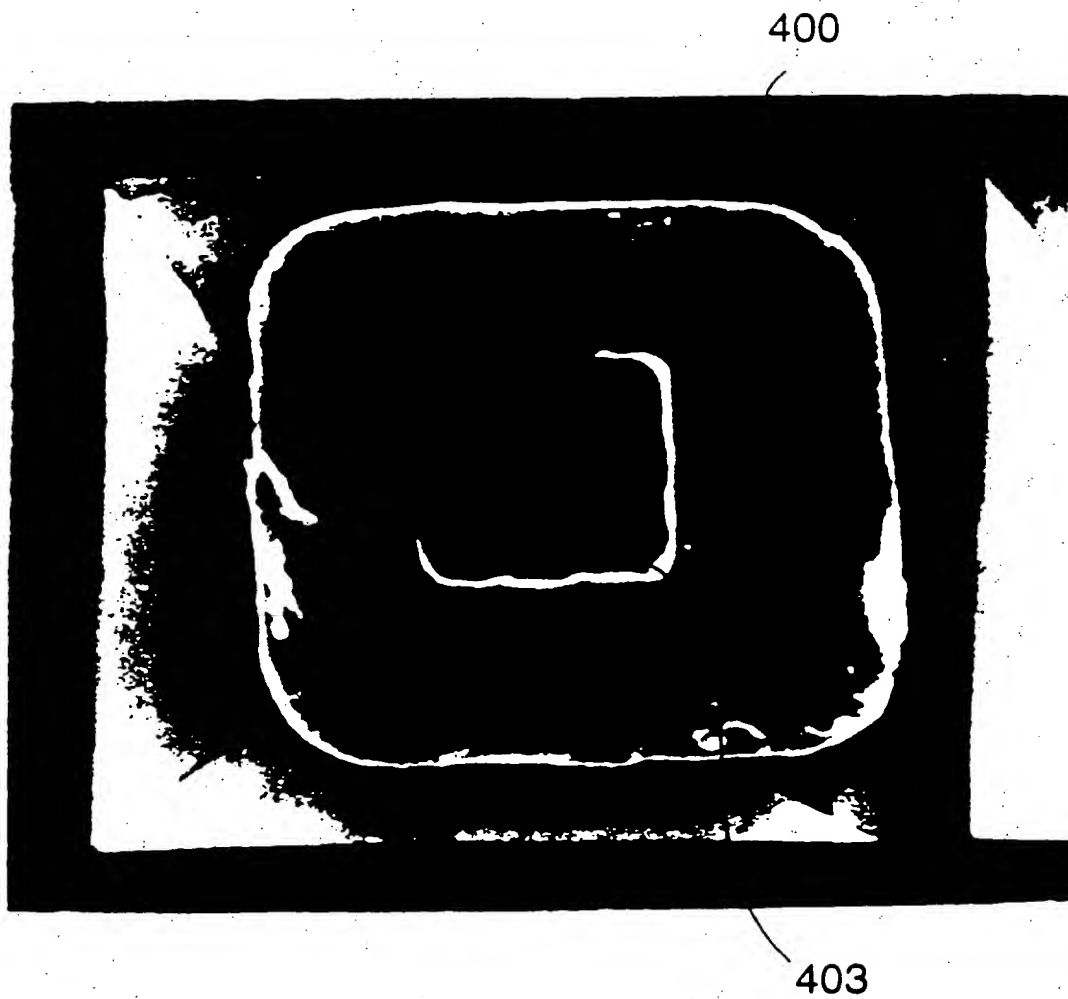
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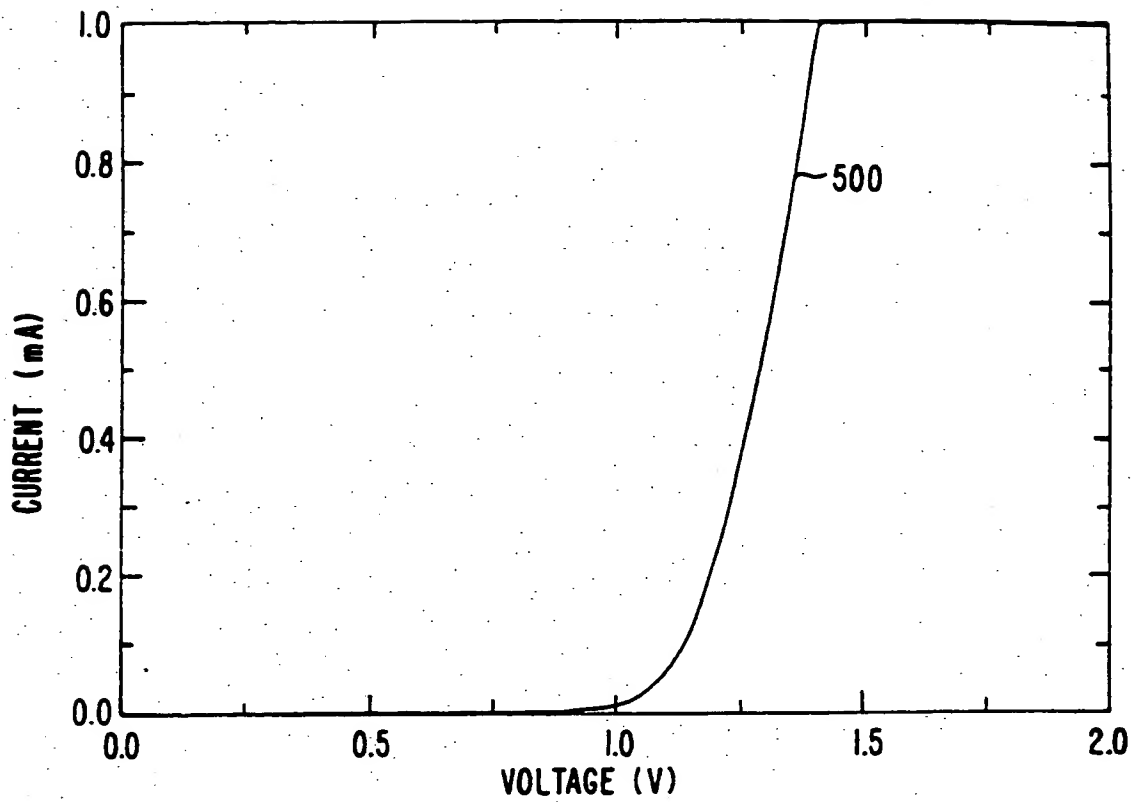
FIG. 16.

FIG. 17.

FIG. 18.

FIG. 19.

FIG. 20.

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FIG. 21.